A Two-Channel Interleaved ADC With Fast-Converging Foreground Time Calibration and Comparison-Based Control Logic

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***Abstract*— A dual-channel interleaved analog-to-digital converter (ADC) operating at 320 MS/s is prototyped to validate a fast-converging foreground time calibration algorithm that is independent of ADC offset errors. An input polarity switching technique is introduced to eliminate the impact of sub-ADC offset mismatches during foreground time calibration. After foreground calibration, the signal-to-noise and distortion ratio (SNDR) and spurious free dynamic range (SFDR) are improved by 8.6 and 18.4 dB, respectively. In the sub-ADC design, a comparison functionality is enabled in the digital circuits to prevent metastability and expedite data conversion. The single-channel conversion rates reach 160 MS/s. The ADC is implemented via 40-nm digital CMOS technology, achieving a 52.01 dB signal-to-noise plus distortion ratio (SNDR) at near-Nyquist input while sampling at 320 MS/s. The overall power consumption is 3.65 mW, which includes an on-chip reference buffer and a clock circuit.**

***Index Terms*— Analog-to-digital converter (ADC), foreground calibration, time-interleaved (TI) ADC, timing-skew mismatch.**

I. Introduction

AS THE interface between analog and digital domains, analog-to-digital converters (ADCs) play a crucial role in various systems, particularly with the proliferation of 5G communication and integrated RF transceiver SOCs in portable devices, necessitating high-speed low-power ADCs [1], [2]. Owing to their cyclic operational mode, single-stage SAR ADCs typically require N comparisons for N-bit resolution. In CMOS technology backward than 28 nm, the sampling frequency of a single-stage single-comparator 10-bit SAR ADC is usually less than 300 MHz [3], [4], [5], [6], [7], [8].

To achieve a sampling rate higher than 300 MHz with 10-bit resolution, timing-interleaved ADC (TI-ADC) with multiple channels has been employed. Introducing parallelism into the time-interleave architecture, along with the low-power consumption characteristic of the SAR structure, enables a balanced trade-off between speed and power [9], [10], [11], [12].

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However, the time-interleaving architecture introduces challenges such as channel mismatches [13], [14], [15], including offset, gain, and timing skew mismatches. Compared with multiple-channel ADCs, a two-channel structure offers relatively easier synchronization and better tolerance to harmonics caused by mismatches [13].

The offset and gain mismatches are independent of the input signal frequency, allowing for direct detection. Conversely, time errors tend to increase with increasing input signal frequency, significantly degrading the ADC dynamic performance [16], [17]. Various calibration methods have been proposed to address the impact of time errors, which can be categorized into foreground and background calibrations. Foreground calibration typically uses additional input signals such as ramp signals or known-frequency sine waves. This calibration offers fast convergence but is unable to track time errors during operation due to voltage and temperature variations [18], [19], [20].

Background calibration involves an additional reference channel or extensive digital computations, leading to slower convergence and significant hardware overhead [9], [10]. In [9], a slope-based time calibration algorithm employing two fully operational ADCs was used to continuously adjust a digitally controllable delay line (DCDL), and the least mean squares (LMS) algorithm was used to converge the time error within a certain range. Furthermore, a sign-equally-based calibration algorithm eliminated the need for an auxiliary ADC for time calibration using the voltage difference between adjacent channels to determine the sign of the signal slope [9]. However, this approach required many samples of a band-limited signal and a reference channel to ensure calibration accuracy. Zero-crossing-based calibration algorithms detect time errors by sensing signal zero-crossing points [23]. However, the voltage comparison cannot distinguish between the comparator offset voltage and voltage error caused by time error, necessitating the elimination of the comparator offset voltage before time calibration [18], [22].

The time calibration process often requires many sampling cycles to extract useful time errors. In applications such as RF receivers, where ADCs are frequently switched ON and OFF to reduce power consumption, ensuring sufficient margin time for time calibration convergence can be challenging. Realistic ADC input signals may prolong the time calibration process, underscoring the need for reliable, fast-converging time

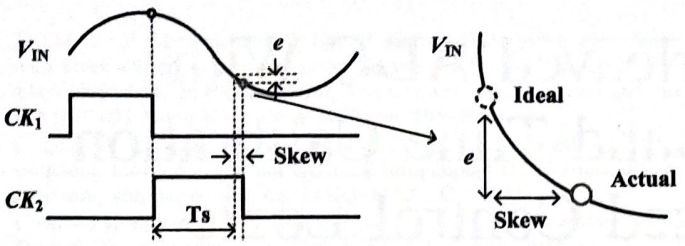


Fig. 1. Sampling error due to timing skews in a TI-ADC.

calibration algorithms suited for intermittent RF transceivers. This article analyzes time mismatches between two identical clock circuits in sub-ADC channels caused by process randomness, temperature, and power supply voltage variations. A foreground time calibration algorithm using the top ADC sampling clock as an input signal is subsequently proposed. By sampling the ADC clock signal, time mismatches are translated into sampled voltage differences, facilitating foreground time correction. Moreover, this method is insensitive to the comparator offset voltage and can simultaneously detect offset and time mismatches between sub-ADC channels. To validate this method, a 10-bit, 320 MS/s dual-channel interleaved ADC is designed.

The article is organized as follows. Section II delineates the sources of the timing skew and its variation with the power supply voltage and temperature. Section III elaborates on the fast-converging foreground calibration algorithm and its implementation details. Section IV describes the circuit implementation of the TI-ADC. The experimental results are presented in Section V. Finally, Section VI summarizes this work.

II. Skew Analysis

Skew refers to the various delays observed from a single clock edge to different positions. In TI-ADC, as shown in Fig. 1, skew typically manifests as the deviation of the sampling interval of two adjacent sub-ADC channels from the ideal sampling interval. Assuming that the ADC input $V_{IN}(t)$ is a sinusoidal signal with an amplitude A_{IN}, the sampling error $e(t)$ can be expressed as [21]

$$e(t) \approx \frac{\delta V_{IN}(t)}{dt} \cdot \Delta t \tag{1}$$

$$= 2 \cdot \pi \cdot F_{IN} \cdot A_{IN} \cdot \cos(2 \cdot \pi \cdot F_{IN} \cdot t) \cdot \Delta t. \tag{2}$$

Here, Δt represents the timing skew, and F_{IN} is the input signal frequency. As the input signal frequency increases, the signal's slope becomes steeper, resulting in a larger sampling error. Consequently, the ADC's dynamic performance significantly deteriorates at higher frequencies. Static mismatches in the routing and devices of different channels cause static skew, whereas variations in the power supply voltage and temperature cause dynamic skew errors.

An inverter serves as a simplified example to elucidate how the power supply and temperature variations impact the propagation delay. As depicted in Fig. 2, the inverter charging process can be likened to the power supply V_{DD} charging the load C_L through the PMOS equivalent resistance R_p, with the NMOS acting as a turn-off switch. By simplifying the model

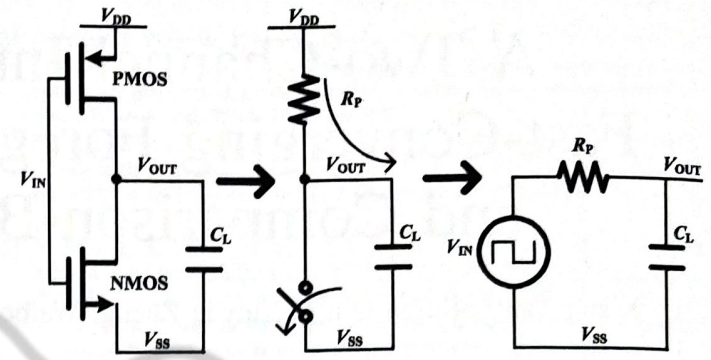


Fig. 2. Model of the inverter charging process.

into a first-order RC network, we obtain

$$V_{IN} = R_P C_L \frac{dV_{OUT}(t)}{dt} + V_{OUT}(t) \tag{3}$$

$$V_{OUT}(t) = (1 - e^{-\frac{t}{R_P C_L}}) V_{IN}. \tag{4}$$

By substituting $V_{OUT}(t) = (V_{DD}/2)$, $V_{IN} = V_{DD}$

$$\frac{V_{DD}}{2} = (i1 - e^{-\frac{t_{pLH}}{R_P C_L}}) j V_{DD} \tag{5}$$

$$t_{pLH} = R_P C_L \ln 2 \approx 0.69 R_P C_L. \tag{6}$$

We then calculate the equivalent resistance of the PMOS transistor during discharging as

$$R_P = \frac{1}{\frac{V_{DD}}{2}} \int_{\frac{V_{DD}}{2}}^{V_{DD}} \frac{V}{I_{DSAT}(1 + \lambda V)} dV$$

$$\approx \frac{3}{4} \frac{V_{DD}}{I_{DSAT}} \left(1 - \frac{7}{9} \lambda V_{DD}\right) \tag{7}$$

$$I_{DSAT} = k'_p \frac{W}{L} ((V_{DD} - V_{Tp}) V_{DSATp} - \frac{V_{DSATp}^2}{\sqrt{2}}) \tag{8}$$

where λ is the channel length modulation coefficient, k'_p is the carrier mobility product of the oxide capacitance per unit area, and V_{DSATp} is the voltage at carrier velocity saturation. Bringing (7) into (6) and ignoring channel length modulation effects, we can obtain

$$t_{pHL} = 0.69 R_p C_L = 0.69 \cdot \frac{3}{4} \frac{C_L V_{DD}}{I_{DSAT}}$$

$$= 0.52 \frac{C_L V_{DD}}{k'_p \frac{W}{L} V_{DSATp} \left(V_{DD} - V_{Tp} - \frac{V_{DSATp}}{2}\right)}. \tag{9}$$

The skew between the two clocks can be expressed as

$$\text{skew} = t_{pHL\_sub1} - t_{pHL\_sub2}. \tag{10}$$

The influence of the power supply voltage and temperature on the skew are assessed below. Suppose that the temperature is fixed such that the power supply voltages of both sub-ADC channels are the same. Equation (10) can be rewritten as

$$\text{skew} = Y(V_{DD}) \cdot \left(\frac{1}{W/L_{sub1}} - \frac{1}{W/L_{sub2}}\right) \tag{11}$$

$$Y(V_{DD}) = \frac{0.52 C_L V_{DD}}{k'_p V_{DSATp} \left(V_{DD} - V_{Tp} - \frac{V_{DSATp}}{2}\right)}. \tag{12}$$

Skew becomes a function of V_{DD} and device size. When there are mismatches between devices, the skew will vary with changes in V_{DD}. The derivative of $Y(V_{DD})$ with respect to V_{DD} decreases as V_{DD} increases

$$\frac{dY(V_{DD})}{dV_{DD}} = \frac{0.52C_L\left(2V_{DD} - V_{Tp} - \frac{V_{DSATp}}{2}\right)}{k'_p V_{DSATp}\left(V_{DD} - V_{Tp} - \frac{V_{DSATp}}{2}\right)^2}. \quad (13)$$

Suppose that the power supply voltage is fixed such that the temperatures of both sub-ADC channels are the same, and that the skew becomes a function of V_{Tp} and the device size. When there are mismatches between devices, the skew varies with changes in temperature, and (10) can be rewritten as

$$\text{skew} = Y(V_{Tp}) \cdot \left(\frac{1}{W/L_{sub1}} - \frac{1}{W/L_{sub2}}\right) \quad (14)$$

$$Y(V_{Tp}) = \frac{0.52C_L V_{DD}}{k'_p V_{DSATp}\left(V_{DD} - V_{Tp} - \frac{V_{DSATp}}{2}\right)}. \quad (15)$$

By calculating the derivative of $Y(V_{Tp})$ with respect to V_{Tp}, we can obtain

$$\frac{dY(V_{Tp})}{dV_{Tp}} = \frac{-0.52C_L V_{DD}}{k'_p V_{DSATp}\left(V_{DD} - V_{Tp} - \frac{V_{DSATp}}{2}\right)^2}. \quad (16)$$

Equations (12) and (15), indicate that the skew is strongly correlated with the power supply voltage and temperature. Another observation from the comparison of (13) and (16) is that the derivative with respect to the power supply voltage is greater than that with respect to temperature.

The above analysis demonstrates the dependence of skew on the power supply voltage and temperature. If the two clock circuits are identical, they will experience the same delay with power supply and temperature variations. However, owing to device and routing mismatches, the two clock circuits exhibit slight differences, causing additional time skew.

The typical clock design implemented in 40-nm CMOS technology serves as an example to illustrate the variation in clock skew under temperature and power supply voltage variations. Simultaneously, the equation approximation based on the process parameters is compared with the simulation results to verify the reliability of the equation.

The first simulation is a Monte Carlo simulation on skew. Fig. 3 shows the results at 25 °C with V_{DD} set to 1.2 V, indicating an average skew of 35.18 fs and a standard deviation of 4.38 ps.

The second simulation illustrates the variation in skew concerning the power supply voltage in the worst cases. As depicted by the blue line with diamonds in Fig. 4, in simulations without a device mismatch, the initial skew at 1.2 V is 0 ps, fluctuating by less than 1 ps within the V_{DD} range of 1–1.4 V. In Monte Carlo simulations considering device mismatch, as shown by the red line with circles in Fig. 4, the initial skew caused by device mismatch is 12 ps. The skew changes by 10 ps when V_{DD} varies from 1 to 1.4 V. The approximate results from the equation are represented by black lines, and the simulation results are in good agreement with the approximate results of the equation. This aligns with prior theoretical analyses.

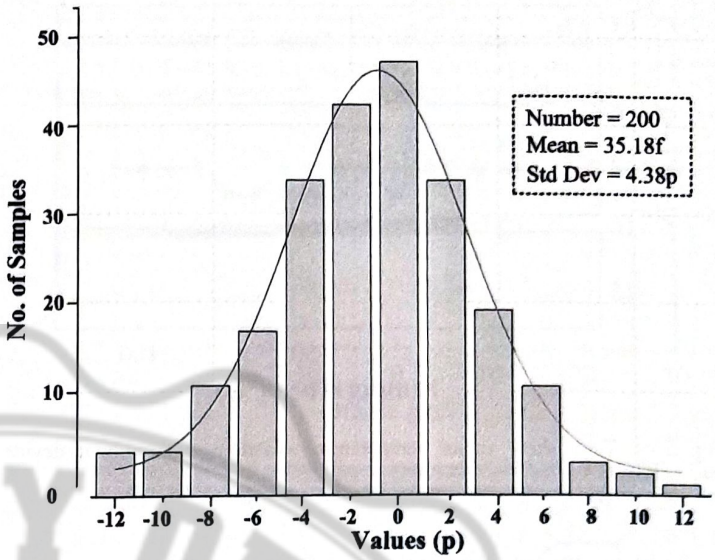


Fig. 3. Monte Carlo simulations showing the skew caused by device mismatch.

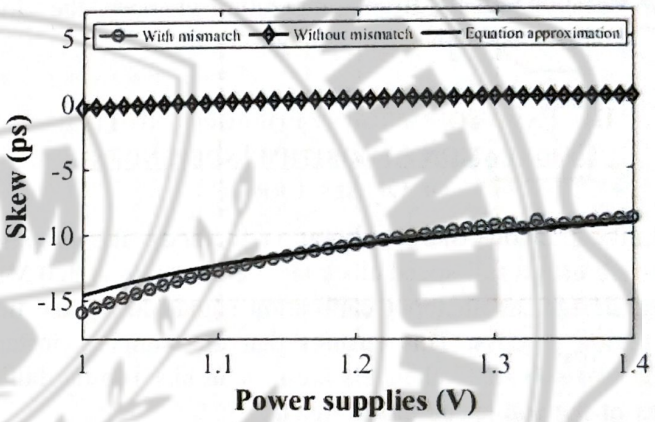


Fig. 4. Time skew versus power supply variations with/without device mismatches.

The third simulation demonstrates the variation in skew with temperature. The simulation results and equation approximation results are shown in Fig. 5. With a real device mismatch, the skew difference remains below 0.3 ps within the range of −40 °C to 125 °C, assuming that the clock circuits for the two sub-ADC channels have the same temperature. This variation is significantly less than the 2 ps required in the 320 MHz design. For a 10-bit ADC, the effective number of bits (ENOB) is typically approximately 9 bits, which means that skew-induced spurs should be below −54 dB. Based on (2), with an input frequency of 160 MHz and a skew of 2 ps, the signal-to-spur power ratio is −54 dB.

Skew is less sensitive to temperature than to the power supply voltage. In practical design, the clock circuits of the two sub-ADC channels are placed together to ensure that they have the same temperature. If the power supplies of the delay lines are regulated by a local LDO, the time skew between the clock generation circuits will remain constant. This method reduces the dynamic component of the time skew, leaving primarily the static component.

On the basis of the analysis presented above, a foreground time calibration method is proposed to address the static skew induced by technology corner variations and random process

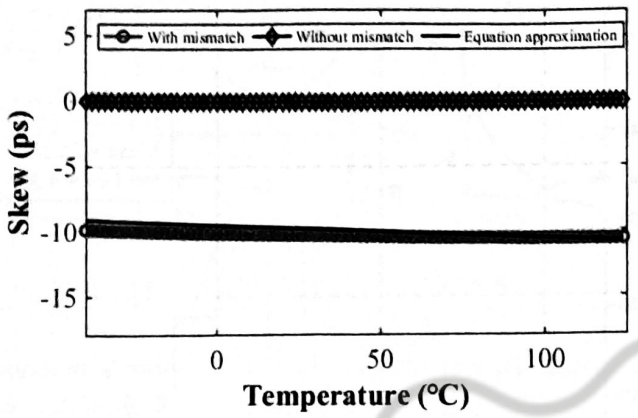


Fig. 5. Time skew versus temperature variations with/without device mismatches.

fluctuations. To mitigate skew variation resulting from voltage fluctuations, a dedicated LDO is employed for the clock tree to ensure a stable power supply. Additionally, to minimize skew variation arising from temperature changes, the clock tree layout is consolidated in a single location.

III. Fast Convergent Foreground Time Calibration Algorithm Independent of Offset Error

Unlike previous skew calibration methods, the proposed approach uses a full-speed clock signal, operating at 320 MHz in the design, as an input calibration signal during the time calibration process. This ensures that the sampling instants of the two sub-ADC channels are synchronized to the falling edges of the full-speed clock signal.

A. Foreground Timing Calibration Algorithm

The primary focus of this method is to utilize a known signal as a reference for the ADC during the foreground calibration process. This approach eliminates the requirement of extra signal generation circuits or external signal sources, as it repurposes the ADC's main clock as the calibration signal. Only a few additional circuits are specifically required for the calibration. The time skew information can be extracted from the digital code of sub-ADC channels.

As illustrated in Fig. 6(a), *CK* represents the main clock of the TI-ADC, a 320-MHz clock signal in this design, repurposed as the input calibration signal for the sub-ADC during the calibration process. *CK*1 and *CK*2 correspond to the 160-MHz sampling clocks of the sub-ADC channels.

In Fig. 6(a), at the *CK*1 and *CK*2 falling edges, sub-ADCs sample the *CK* at the falling edge, respectively, and the two sub-ADC sampling points are assumed to be in the middle of *CK* in. Currently, the output codes of the two sub-ADC channels can be expressed as

$$\mathrm{DOUT}_{\mathrm{sub1}} = \mathrm{DOUT}_{\mathrm{sub2}} = \frac{V_{\mathrm{DD}}}{2 * V_{\mathrm{REF}}} * 2^N. \tag{17}$$

N is the ADC resolution. In this scenario, there is no time skew, i.e., $\Delta t = 0$, and the difference between the two sub-ADC outputs is $\Delta V = 0$.

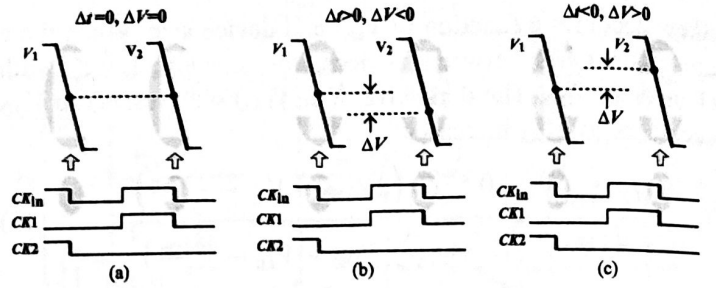


Fig. 6. Sub-ADC channels without offset sampling the buffered clock falling edge: (a) no time skew, (b) sub-ADC$_2$ lags behind sub-ADC$_1$, and (c) sub-ADC$_2$ leads ahead sub-ADC$_1$.

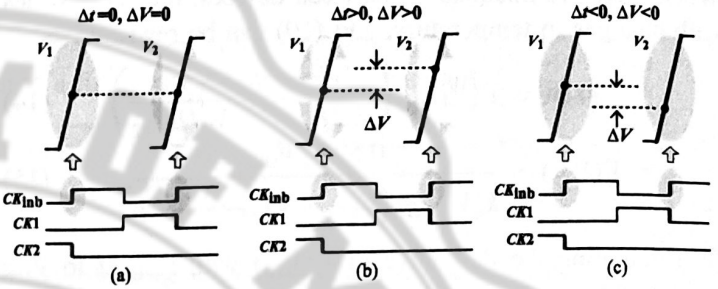


Fig. 7. Sub-ADC channels without offset sampling the buffered clock rising edge: (a) no time skew, (b) sub-ADC$_2$ lags behind sub-ADC$_1$, and (c) sub-ADC$_2$ leads ahead sub-ADC$_1$.

As shown in Fig. 6(a), assuming that sub-ADC$_1$ still samples at the middle of *CK* in and that sub-ADC$_2$ has a time skew of $\pm\Delta t$, the output result of sub-ADC$_2$ can be expressed as

$$\mathrm{DOUT}_{\mathrm{sub2}} = \frac{V_{\mathrm{DD}}}{2 * V_{\mathrm{REF}}} * 2^N + (K * \Delta t)_{\mathrm{digi}}. \tag{18}$$

K represents the voltage slope of *CK* in. In this way, the time skew is converted to the digital code difference $(K * \Delta t)_{\mathrm{digi}}$, which can be used as the skew indicator for a time calibration algorithm to correct the time skew.

Unfortunately, even if there is no time skew, the offset mismatch between two sub-ADC channels will also generate the output difference. As shown in Fig. 7(b), there is no time skew, but sub-ADC$_2$ has an offset error $V_{\mathrm{off.2}}$, which is directly shown as the output code difference. In Fig. 7(c), sub-ADC$_2$ has both time error and offset error. At this time, its output can be expressed as

$$\mathrm{DOUT}_{\mathrm{sub2}} = \frac{V_{\mathrm{DD}}}{2 * V_{\mathrm{REF}}} * 2^N + (K * \Delta t)_{\mathrm{digi}} + (\mathrm{offset2})_{\mathrm{digi}}. \tag{19}$$

The difference between the two sub-ADC output codes contains two types of errors: offset and time skew. Therefore, it cannot accurately guide time mismatch calibration.

B. Input Polarity Switching Technique

An input polarity switching technique is proposed to differentiate the output errors caused by time skew and offset mismatch. When sub-ADC$_2$ samples the falling edge of *CK* in, as shown in Fig. 8(b), the slope K of the signal is negative.

Assume that the input signal polarity can be reversed. As shown in Fig. 9(b), sub-ADC$_2$ samples the rising edge of *CK* in, and the sign of the slope K also reverses and becomes

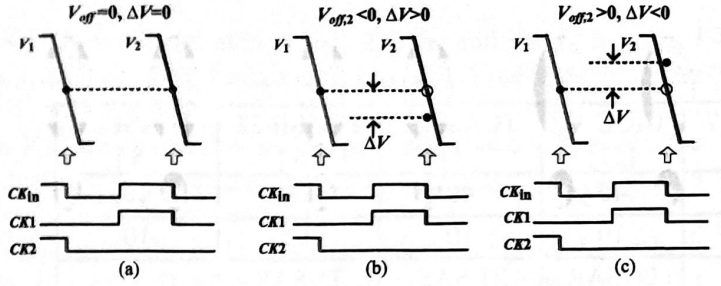


Fig. 8. Sub-ADC channels without skew but with offset sampling the buffered clock falling edge: (a) no offset, (b) sub-ADC$_2$ with negative offset, and (c) sub-ADC$_2$ with positive offset.

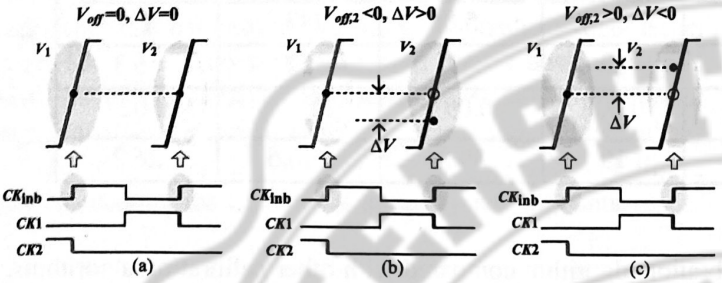


Fig. 9. Sub-ADC channels without skew but with offset sampling the buffered clock rising edge: (a) no offset, (b) sub-ADC$_2$ with negative offset, and (c) sub-ADC$_2$ with positive offset.

positive. The output results of sub-ADC$_2$ in the original and reversed cases are expressed as

$$\mathrm{DOUT}_{\mathrm{sub2\_rise}} = \frac{V_{\mathrm{DD}}}{2 * V_{\mathrm{REF}}} * 2^N + (K * \Delta t)_{\mathrm{digi}} + (\mathrm{offset2})_{\mathrm{digi}} \quad (20)$$

$$\mathrm{DOUT}_{\mathrm{sub2\_fall}} = \frac{V_{\mathrm{DD}}}{2 * V_{\mathrm{REF}}} * 2^N - (K * \Delta t)_{\mathrm{digi}} + (\mathrm{offset2})_{\mathrm{digi}}. \quad (21)$$

In the two results, the error magnitudes related to the time skew are equal, and the signs are opposite, whereas the error magnitudes related to offset are the same. Therefore, subtracting the two conversion results can eliminate the offset and only retain the skew information, while adding the two conversion results can obtain the offset information. Using the input signal polarity switching method, time skew and offset mismatch can be accurately extracted.

The simulation comparison results are shown in Fig. 10. The comparison highlights the residue skew after calibration with and without using the input polarity switching technique. The initial skew was set to 5 ps. When the input polarity switching technique is not used, as indicated by the red line, the residue skew after calibration is related to the sub-ADC's offset because the offset error mixes with the voltage error caused by the skew. Conversely, the blue line represents the residue skew after using the input polarity switching technique, showing that it remains within the minimum step size of the DCDL. This finding demonstrates that the input polarity switching technique effectively isolates the offset influence, allowing for accurate skew calibration.

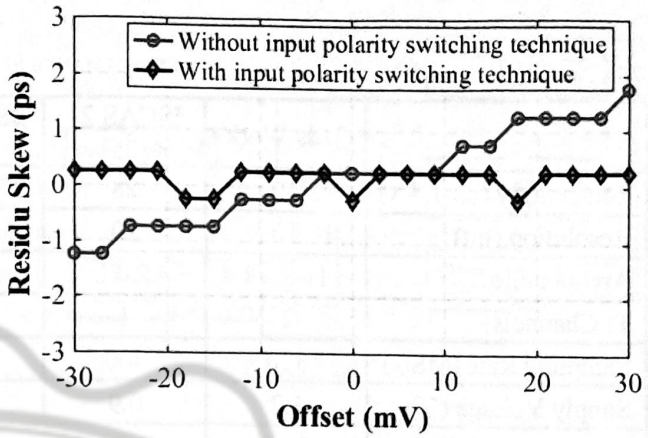


Fig. 10. Residue skew after foreground calibration with the Sub-ADC offset.

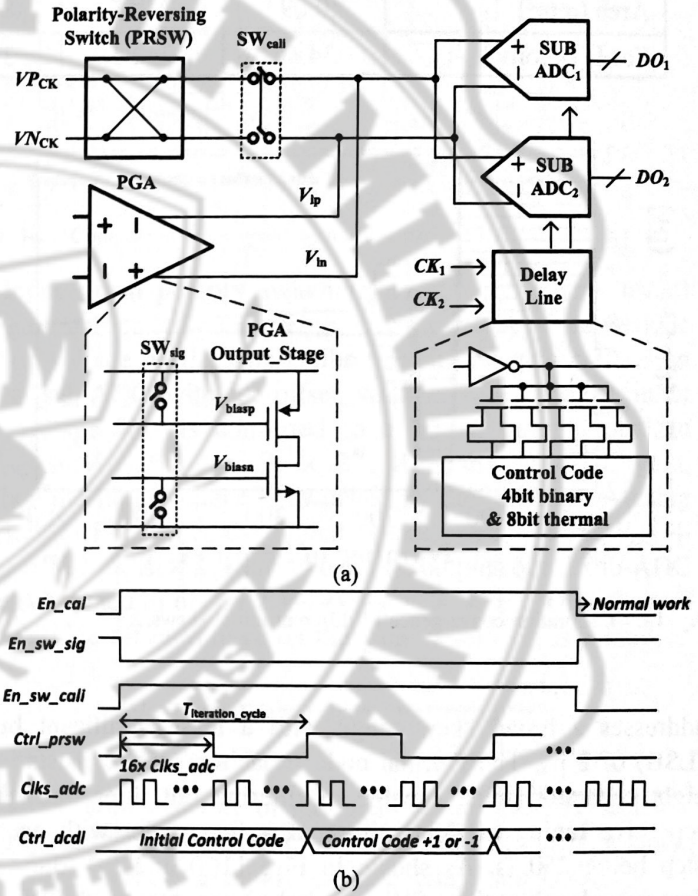


Fig. 11. (a) Schematic of the ADC input connection and detailed implementation of the calibration circuit. (b) Timing diagram of the calibration and normal operations.

C. Foreground Timing Calibration Circuits

The foreground calibration circuit consists of two main parts, as shown in Fig. 11(a). One part is the delay line for compensating for time mismatches, and the other part is the auxiliary calibration circuit, which includes input polarity reversal switches (PRSW) and two sets of switches SWcali and SWsig.

The two sub-ADC channels are controlled by two clock signals from the delay lines. The DCDL provides a calibration range of 32 ps, approximately 1% of the sampling period. It comprises a 4-bit binary-weighted capacitor array and an 8-bit thermal code capacitor array. The binary-weighted array

TABLE I
PERFORMANCE SUMMARY AND COMPARISON

	This Work	ISCAS 21 [25]	JSSC 17 [26]	CICC 17 [27]	TCASI 22 [7]	TCASII 22 [6]	TCASI 22 [8]
Technology (nm)	40	28	65	40	40	28	40
Resolution (bit)	10	10	11	10	10	12	10
Architecture	TI-SAR	SAR-Flash	SAR	2b SAR	TI-SAR	TI-SAR	SAR
TI Channels	2	1	1	1	4	6	1
Sampling Rate (MS/s)	320	400	100	300	500	900	100
Supply Voltage (V)	1.2	0.9	1.2	1.2	1.1/0.9	1/1.2	1/1.3
Power (mW)	3.65	4.55	2.44	2.1	5.8	43	1.4
SNDR (dB)	52	45.2	57.93	53	51	52	56.3
Area (mm^2)	0.09	0.011	0.012	0.008	0.093	0.48	0.027
FoM (fJ/conv.)	34.46	74.83	37.9	19	39.8	146.6	26.2

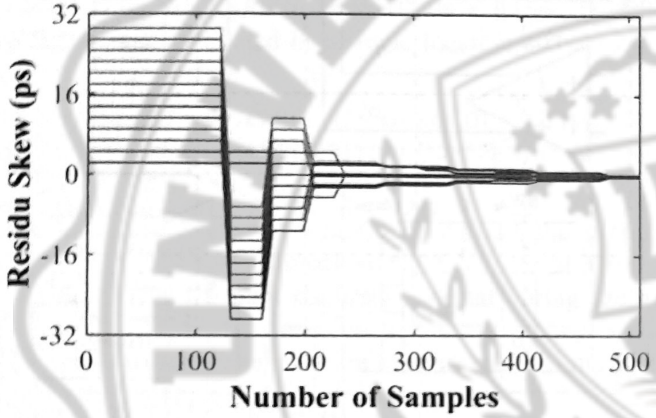


Fig. 12. Calibration convergence of different initial skews.

addresses a broad skew range with a least significant bit (LSB) of 2 ps. The thermal code capacitor array consists of eight capacitor units, capable of filtering out jitter through repetitive tuning of delay times at a fine scale, with each step being 250 fs. As shown in Fig. 11(a) and (b), during foreground calibration, SW_{sig} switches are OFF, and SW_{cali} switches are ON, allowing the calibration signals VP_{CK} and VN_{CK} to enter the TI-ADC through the polarity-reversing switch. When Ctrl_prsw is high, the PRSW is in positive polarity, and the sub-ADC channels alternately digitize the calibration signal 16 times. Then, the PRSW switches to negative polarity for another 16 times. This completes an iteration, updating the DCDL control word Ctrl_dcdl via (20) and (21). The DCDL uses a 12-bit control word, necessitating 12 iteration cycles for full foreground calibration, with each cycle comprising 32 ADC conversions. As shown in Fig. 12, the simulation results demonstrate the final convergence of the foreground calibration with a skew of approximately 1% of the sampling period. This design adopts a combination of binary and thermal codes, first coarse adjustment and then fine adjustment, and because it has fewer iterations while meeting the calibration range, the calibration converges quickly. Table I shows the convergence speed of the proposed foreground calibration algorithm compared with other calibration algorithms. After foreground calibration, SWsig switches are turned on and SWcali switches are turned off, enabling the TI-ADC to digitize input signals from the programmable gain amplifier (PGA).

D. Concerns in the Foreground Timing Calibration

As depicted in Fig. 11(a), a noteworthy consideration in the proposed foreground timing calibration is the inclusion of an additional switch, SWsig, within the signal path. The variability in the ON-state resistance of the switch with signal amplitude could impact signal linearity due to the IR voltage drop, whereas the presence of parasitic capacitance may impose demands on the PGA's driving capability. In the actual analog front-end circuit, SWsig is implemented as a disabled switch. During timing calibration, when the signal path must be inactive, the PGA is disabled, and its output is left floating. In operational mode, the calibration switch SWcali turns off, ensuring that there are no charge injection or clock-through effects.

Throughout the foreground time calibration process, the routing of the calibration clock signal plays a crucial role in determining the accuracy of the timing calibration. However, there exists a trade-off in the routing of the calibration clock signal. While wider metal lines result in reduced routing mismatches, they also introduce greater parasitic capacitance to the substrate. This additional capacitance can slow both the calibration clock signal during timing calibration and the real input signal during the operational mode. To mitigate these effects, three metal layers are stacked to minimize parasitic resistance and mutual mismatches. Furthermore, both sides of the calibration clock signal are shielded by GND lines to minimize crosstalk.

The impact of GND shielding parasitic capacitance on the sharpness of the calibration signal edge is a concern. For the calibration algorithm to accurately determine if the sampling clock is leading or lagging, the voltage difference created by the slope multiplied by the smallest time step of the DCDL must exceed the ADC's LSB voltage. In this design, the

DCDL's minimum step size is 250 fs, and the LSB voltage is 2 mV, requiring a minimum slope of 8 V/ns. Assuming that the calibration signal edge is a ramp signal, a change from V_{SS} to V_{DD} which is 1.2 V in 150 ps is still much longer than the edge time of the calibration signal. Therefore, the calibration precision requirements are met.

Equations (20) and (21) assume identical slopes, K, for both the rise and fall edges. However, practical chips can exhibit output impedance mismatches between PMOS and NMOS transistors driving the calibration signal, leading to differing slopes for rise and fall edges. This discrepancy can cause varying voltages to be sampled by the ADC at these edges, impacting the calibration accuracy. To address this issue, larger MOS transistors are employed in this design to drive ADC sampling. These larger transistors exhibit lower output impedances, mitigating the effects of resistance mismatches and ensuring minimal variation in the rise and fall times, thereby meeting the calibration accuracy requirements.

E. Foreground Offset and Gain Calibration

Foreground calibration includes offset calibration, gain calibration, and timing calibration. Typically, timing calibration is performed after offset and gain calibrations. This sequence is preferred because the ADC offset and gain mismatches can significantly influence timing calibration, whereas the ADC time skew does not necessarily impact offset and gain calibration at low frequencies.

The offset error mainly originates from device mismatches in the comparator. To reduce the kickback issue caused by parasitic capacitance at the input of the comparator and the nonlinearity of input parasitic capacitance with common-mode variation, the size of the input transistors of the comparator is small, resulting in a large offset.

The gain of the SAR ADCs is primarily determined by the reference voltage and the ratio of the DAC capacitance to the parasitic capacitance. Typically, reference voltage generation circuits include reference voltage generation and reference voltage buffers. To reduce mutual interference between reference voltages in channels, different buffers biased by the same reference are placed near each channel. Mismatch in the buffers and threshold voltage deviation introduces gain error. The foreground calibrations for offset and gain are similar to the method in [24]. When calibrating the offset, the calibration signals VP_{CK} and VN_{CK} are simultaneously connected to the common-mode voltage. The ADC output codes are accumulated and averaged to obtain the offset information for each channel. When calibrating the gain, the calibration signal VP_{CK} is connected to V_{REFP}, VN_{CK} is connected to V_{REFN}, and a dc voltage is applied to the ADC input. The ADC output codes are accumulated and averaged and then compared with the ideal input $V_{REFP} - V_{REFN}$ to obtain gain error information. Notably, during offset calibration, mismatches exist in the input switch IR drop and the positive and negative terminal DACs, resulting in minor offset errors even after calibration. For gain calibration, it is necessary to use positive and negative dc signals separately for calibration, and then average the calibration results to ensure better calibration accuracy.

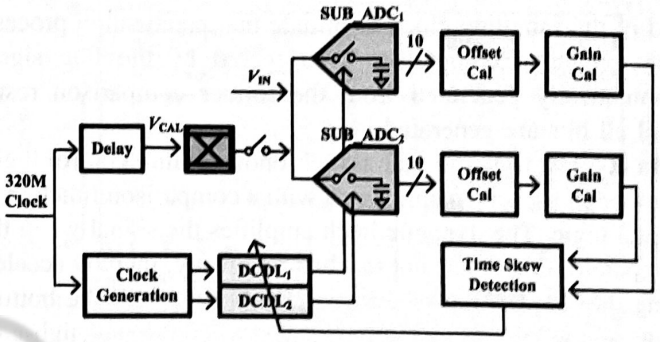


Fig. 13. Two-channel 10-bit 320MS/s TI-ADC.

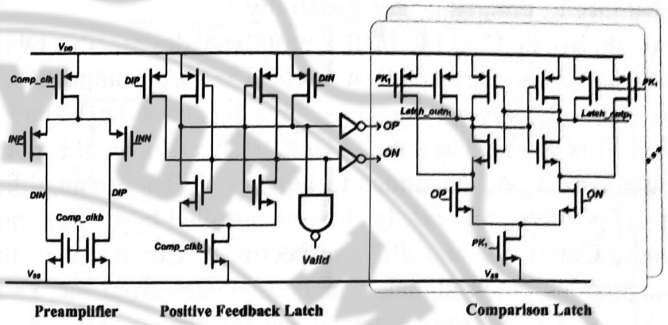


Fig. 14. Comparator codesigned with a comparison latch.

Input signal polarity switching technology is very useful in gain calibration. It can eliminate the effect of the residue offset voltage on the gain calibration. In the gain calibration of a sub-ADC with an offset voltage V_{OFF}, and an input dc voltage V_{DC} is converted to a digital output equal to $(V_{DC} + V_{OFF})/V_{REF} \times A \times 2^N$. A is the sub-ADC gain. When the input voltage is switched by the polarity reversing switch in Fig. 11(a), the digital output is equal to $(-V_{DC} + V_{OFF})/V_{REF} \times A \times 2^N$. The two digital outputs of the sub-ADC are subtracted to obtain $2\ V_{DC}/V_{REF} \times A \times 2^N$. The effect of the residue offset voltage on the gain calibration is removed.

IV. Two-Way Interleaved ADC

A. Two-Way Interleaved Structure

The overall structure of the dual-channel ADC is depicted in Fig. 13, which consists of two sub-ADC channels, a clock generation block, a digital control delay line (DCDL), an offset and gain calibration module, and a time skew detection module. The sub-ADC channels have two input sources: one is the PGA output, and the other is the calibration signal V_{CAL} for detecting the timing skew. The calibration signal V_{CAL} is generated by the main 320 MHz system clock delay and is fed into the ADC after passing through the input signal polarity switch.

In the foreground calibration, the final stage of the front-end PGA is turned off. The sub-ADC performs offset calibration first, then gain calibration, and finally time skew calibration.

B. SAR ADC Comparison-Based Control Logic

Asynchronous control logic is commonly employed in high-speed SAR-ADCs because of its efficient time utilization and elimination of high-power high-speed clocks. The asynchronous digital circuit implements sequential control logic. Only the first comparison is synchronously triggered by the

end of the sampling clock to initiate the quantization process. The remaining comparison is triggered by the flag signal automatically generated from the former comparison result until all bits are generated.

In contrast to traditional asynchronous timing control logic, this design uses a dynamic latch with a comparison function in digital logic. The dynamic latch amplifies the signal when the comparator output has not reached full swing, thereby accelerating the propagation of the comparator output to the bottom plate of the capacitor. Furthermore, the additional high-gain positive feedback in the dynamic latch further reduces the probability of comparator metastability.

As shown in Fig. 14, in the prototype design, the DFFs are replaced by a comparison latch. The DAC output flows in a dynamic preamplifier, a positive feedback latch, and a comparison latch. The comparison latch takes in the comparator output and continues to amplify it. The preamplifier and the positive feedback latch are controlled by two internal signals, Comp_clk and PK_i, respectively. Comp_clk is the asynchronous clock signal, which originates from the Valid signal, and PK_i is from Asyn_clk$_i$ in Fig. 15.

In an N-bit ADC, a typical comparator needs to drive at least N DFFs that have a large input capacitance. In the layout, the comparator output routes a long path to connect the entire digital control logic, which causes heavy parasitic capacitance. Thus, the comparator latch output is followed by two inverters. The comparator output only enters a NAND gate to generate a Valid signal, whereas the inverters' outputs drive the comparison latches. Owing to the heavy parasitic capacitance, the falling and rising edges are normally slow. The comparison latch makes use of the differential signal, OP and ON, to speed up signal propagation and avoid metastability. Notably, the ith comparison latch is not triggered by Asyc_clk$_i$ but by Asyc_clk$_{(i-1)}$. Before the comparator latch in the current bit cycle is ready.

The proposed latch comparison has several merits. First, the comparator saves time by reducing the needed amplitude swing. Second, both comparator differential terminals are used to speed up signal propagation.

As shown in Fig. 15, the ADC completes sampling on the falling edge of the sampling clock Samp_clk. After a digital logic delay of t_{logic}, the falling edge of the comparator clock Comp_clk is generated. Simultaneously, the falling edge of the sampling clock also generates the rising edge of the asynchronous clock Asyc_clk$_1$.

A comparison period begins at the falling edge of Comp_clk. After a time t_{comp}, the comparator compares the polarity of the input signal. Notably, the comparator output does not fully settle to rail-to-rail. At this point, the two signal paths are separated. As indicated by the red dotted arrows in the diagram, in one of the paths, the output Comp_out of the comparator positive feedback latch is captured by a comparison latch after a time t_{latch} and is amplified to full swing. The output of the comparison latch will drive the bottom plate of the capacitor to begin settling. The time taken for the DAC settling is denoted as T_{DAC}. This path is referred to as the DAC settling path. In the other path, the comparator output first enters a NAND gate to generate a rising edge

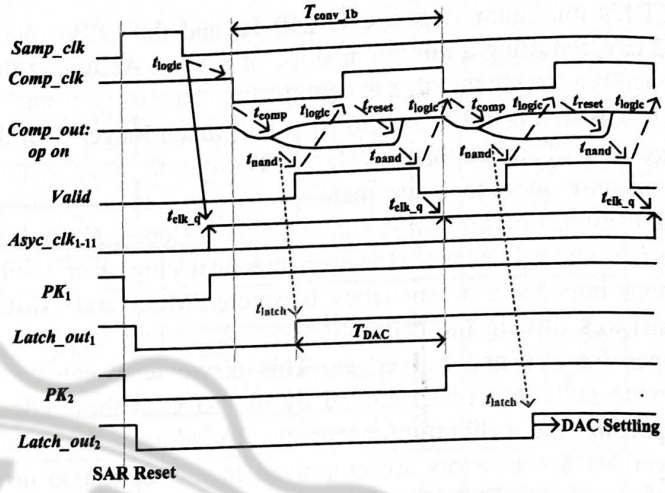


Fig. 15. Internal signals in digital control logic.

of Valid, indicating the completion of the comparison. Then, Valid passes through a digital logic delay of t_{logic} to trigger the rising edge of Comp_clk for the comparator reset. Afterward, the comparator is reset for a time t_{reset}, and both op-amps return to a high state. The comparator output subsequently passes through a time t_{nand} to generate a falling edge of Valid, indicating the completion of the comparator reset. Finally, Valid triggers the falling edge of Comp_clk to start the next comparison cycle after a digital logic delay of t_{logic}. This path is referred to as the comparator control path.

A complete conversion cycle time can be expressed as

$$T_{\text{conv\_1b}} = t_{\text{comp}} + t_{\text{reset}} + 2 * t_{\text{nand}} + 2 * t_{\text{logic}}. \tag{22}$$

The time used for the DAC to settle can be expressed as

$$T_{\text{DAC}} = T_{\text{conv\_1b}} - t_{\text{comp}} - t_{\text{latch}}. \tag{23}$$

In typical designs, multiple DFFs are used to latch the comparator results. The comparator output may fail to be captured by DFFs because it does not settle to rail-to-rail which may cause short-circuit currents in the DFFs and potential metastability issues. Furthermore, Valid is used to drive at least N DFFs, and excessive parasitic capacitance would increase the t_{nand} time, thereby increasing the conversion period $T_{\text{conv\_1b}}$, which is a significant waste for ADCs requiring N conversions. Additionally, in typical designs, the comparator results must be captured by DFFs before controlling the capacitor array, which further reduces the time for DAC settling, limiting the ADC conversion rate. Overall, typical designs involve a tight balance between speed, power consumption, and metastability.

In this design, the comparator's output does not need to wait for the DFFs to capture; instead, the comparison latch is enabled in advance, and the comparison function is utilized to accelerate the transmission of the comparison results to the bottom plate of the capacitor. This reduces the delay of the DAC settling path and avoids the occurrence of metastability.

V. Measurement Results

The prototype of the two-way interleaved ADC is fabricated via 40-nm CMOS technology with a 1.2-V supply voltage. Fig. 16 shows a chip photograph of the proposed ADC and

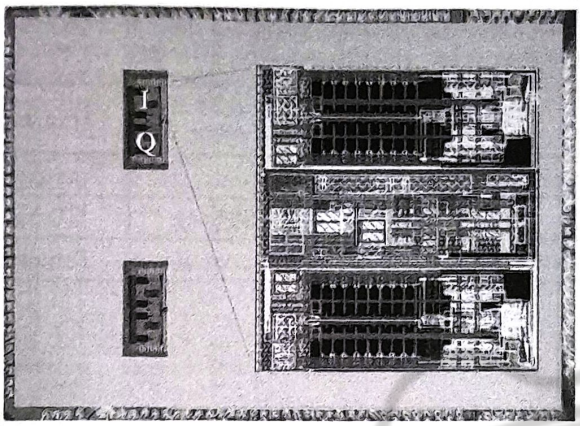


Fig. 16. Chip photograph and zoomed-in layout.

a zoomed-in layout view. The design is integrated into a receiver and the interleaved ADC occupies 210 μm × 230 μm, including a fully on-chip offset, gain, and skew foreground calibration engine. The sub-ADC core is only 210 μm × 80 μm. The unit capacitance in the C-DAC is approximately 1 fF for the MOM capacitor. The reference voltage buffer, clock generation circuit, and calibration circuit are located between the two sub-ADC channels.

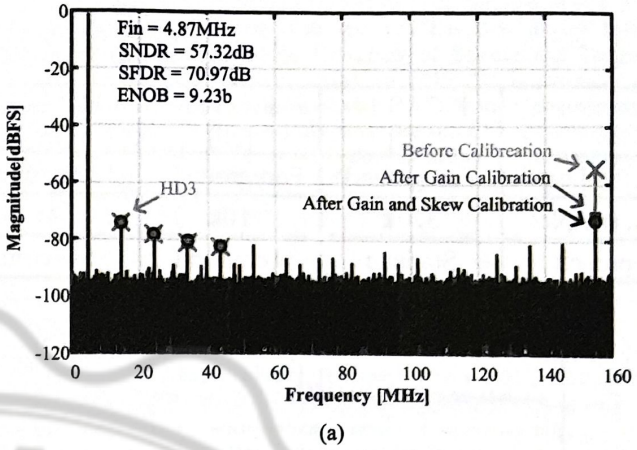
This design addresses inter-channel mismatch by employing various calibration methods. To demonstrate the effects of different calibrations, the calibration circuits can be separately activated through the register during testing. Both gain error and timing error are signal-dependent, and tones produced by both mismatches occur at the same frequency in the ADC output spectrum. To differentiate the effects of gain error and timing skew on the ADC, different frequency sinusoidal signals are used. With low-frequency inputs, the skew has almost no effect on the ADC performance. The ADC performances with/without gain calibration can be used to evaluate the gain calibration.

The gain mismatches must be corrected before the skew calibration. As the input signal frequency increases, the ADC performance degrades due to the skew. With a high-frequency input signal, the measurement results with/without timing calibration are compared to manifest the timing calibration.

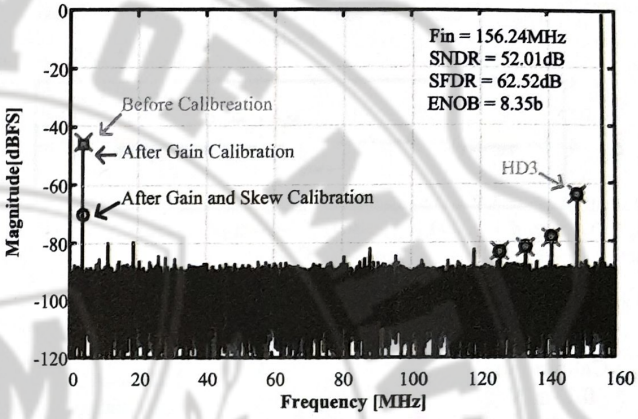
Since the ADC is integrated into the receiver, to independently test the performance of the ADC, a MUX is connected in parallel to the ADC input, leading to two dedicated test pins. The MUX adopts 3.3 V devices to ensure the linearity of the input signal. The sine wave signal is generated by a signal source and driven into the ADC via a buffer on the test board.

Fig. 17(a) depicts the spectrum of the ADC measured at a sampling frequency of 320 MHz with an input signal of 4.87 MHz and 1.8 V_{P-P} differential sinusoidal inputs. The measured signal-to-noise and distortion ratio (SNDR) and spurious free dynamic range (SFDR) are 57.32 and 70.97 dB, respectively. At this frequency, the impact of time mismatch on the ADC is negligible. The one caused by the gain mismatch is reduced from 53.14 to 70.97 dB after the gain calibration.

Fig. 17(b) shows the ADC output spectrum with an input signal frequency equal to 156.24 MHz. Without any calibration, the measured SNDR and SFDR are 43.45 and 44.06 dB,



(a)



(b)

Fig. 17. Measured spectrum at (a) input signal frequency (F_{in}) = 2 MHz and (b) F_{in} = 159 MHz with sampling frequency (F_s) = 320 MHz.

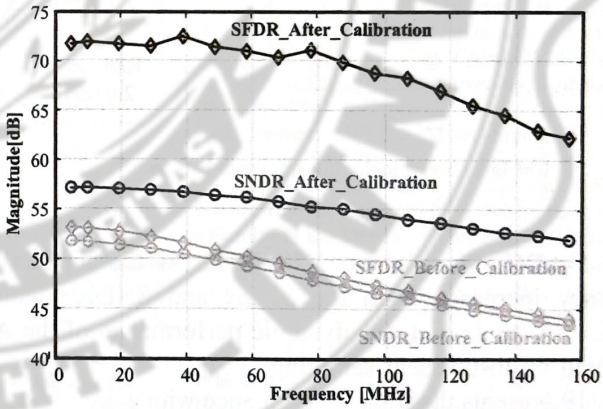


Fig. 18. Measured SNDR and SFDR versus the F_{in} at F_s = 320 MS/s.

respectively. After the gain calibration, the measured SNDR and SFDR are 43.91 and 44.61 dB, respectively. The tone at the $F_s/2-F_{in}$ frequency does not significantly improve because the interchannel time mismatch is still present. After time calibration, the SFDR improves from 44.06 to 62.52 dB, and the tones caused by mismatch are reduced below the third harmonic. The third harmonic may be caused inside one channel ADC by two factors: capacitor mismatches in C-DAC and insufficient settling during sampling. Fig. 18 shows the variations in the SNDR and SFDR with the input signal frequency. When the input signal frequency is less than 50 MHz, both the SFDR and SNDR remain relatively constant. In this range, the SFDR is limited primarily by the third harmonic caused by C-DAC capacitor mismatches in

TABLE II
CONVERGENCE SPEED COMPARISON

	ISCAS 14 [22]	JSSC 17 [28]	TCASI 20 [29]	TCASI 21 [30]	TCASI 22 [31]	TCASI 23 [32]	This work
Method type	Foreground	Foreground	Foreground	Foreground	Background	Foreground	Foreground
No. samples	320k	10k	4k	330k	110k	100*64k	0.5k
Approach	Statistic	Temporal	Spectral	Temporal	Temporal	Spectral	Temporal

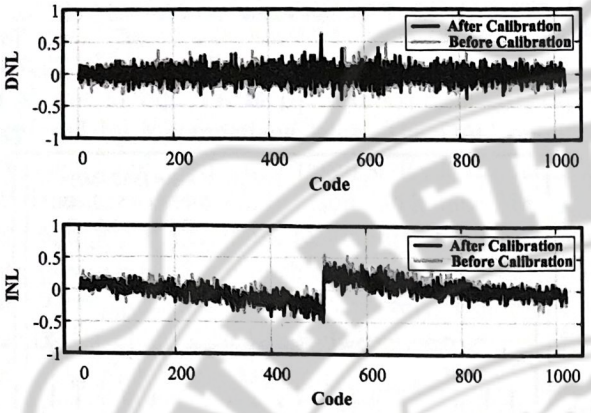


Fig. 19. Measured DNL and INL.

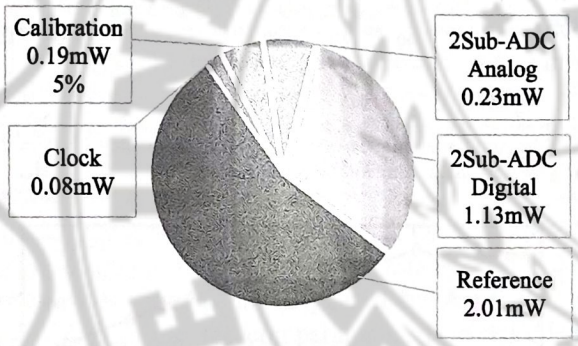


Fig. 20. Power breakdown including reference buffers.

one sub-ADC. Starting from 50 MHz, as the input signal frequency increases, both the SFDR and SNDR gradually decrease. At this point, the dynamic performance of the ADC is limited by insufficient sampling.

Fig. 19 presents the static performance with a 4.87 MHz sine wave as the input. The maximum DNL is −0.38/0.60 LSB, and the INL is −0.48/0.43 LSB. The significant jumps in DNL may be attributed to the parasitic nature of the MSB capacitor in the C-DAC. The total ADC power consumption at a 1.2 V power supply voltage and a 320 MS/s sampling rate is 3.65 mW. As shown in Fig. 20, in the simulated power breakdown, the calibration circuit consumes only 5% during one-time calibration, two sub-ADCs consume 19%, the reference circuit consumes 55%, and the clock generation circuit and other circuits consume 2%. This design adopts an on-chip voltage follower scheme for the reference buffer, resulting in faster settling and a stable reference voltage at the expense of higher power consumption. Overall, this work has achieved a Walden FoM of 34.46-fJ/conversion step at the Nyquist frequency. In Table II, ADC performance is compared with the state-of-the-art ADCs.

VI. CONCLUSION

This article introduces a foreground calibration technique based on polarity switching of the input clock signal, achieving calibration results that are immune to offset errors and fast convergence. The tone caused by the skew is reduced from −46 to −70 dB. This design uses a dynamic latch with a comparison function in the digital circuitry to prevent metastability and expedite data conversion, achieving a single-channel conversion speed of 160 MS/s. Leveraging the introduced calibration technique and fast single-channel conversion, a 10-bit 320 MS/s ADC achieves an ENOB of 9.29 b for low-frequency input signals and 8.38 b for high-frequency input signals.

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