

The Error Analysis of Bit Weight Self-Calibration Methods for High-Resolution SAR ADCs

Yanhang Chen[✉], Graduate Student Member, IEEE, Siji Huang[✉], Student Member, IEEE, Qifeng Huang[✉], Member, IEEE, Yifei Fan[✉], Member, IEEE, and Jie Yuan[✉], Senior Member, IEEE

Abstract—High-resolution successive approximation register (SAR) analog-to-digital converters (ADCs) commonly need to calibrate their bit weights. Due to the nonidealities of the calibration circuits, the calibrated bit weights carry errors. This error could propagate during the calibration procedure. Due to the high precision requirement of these ADCs, such residue error commonly becomes the signal-to-noise-and-distortion ratio (SNDR) bottleneck of the overall ADC. This article presents an analysis of the residue error from bit weight self-calibration methods of high-resolution SAR ADCs. The major sources contributing to this error and the error reduction methods are quantitatively analyzed. A statistical analysis of the noise-induced random error is developed. Our statistical model finds that the noise-induced random error follows the chi-square distribution. In practice, this random error is commonly reduced by repetitively measuring and averaging the calibrated bit weights. Our statistical model quantifies this bit weight error and leads to a clearer understanding of the error mechanism and design trade-offs. Following our chi-square model, the SNDR degradation due to the circuit noise during the calibration can be easily estimated without going through the time-consuming traditional transistor-level design and simulation process. The required repetition time can also be calculated. The bit-weight error models derived in this article are verified with measurement on a 16-bit SAR ADC design in a 180-nm CMOS process. Results from our model match both simulations and measurements well.

Index Terms—Bit weight calibration, calibration error, error model, high-resolution successive approximation register (SAR) analog-to-digital converter (ADC), statistical error analysis.

I. INTRODUCTION

SUCCESSIVE approximation register (SAR) analog-to-digital converter (ADC) based on the capacitive digital-to-analog converter (CDAC) has become widely used in recent years for its highly digital operation, compactness, and low power consumption [1], [2], [3], [4], [5]. The bit weight error of the CDAC due to capacitor mismatch and parasitic becomes an important bottleneck and thus bit weight calibration is usually required in SAR ADCs. Among different calibration techniques, the foreground bit weight self-calibration has high popularity since it only requires a simple

digital algorithm with small circuit overhead as it reuses the SAR ADC core circuits and requires no special off-chip component or trimming [6], [7], [8], [9], [10], [11], [12]. Hence, it finds wide applications in various SAR ADCs, such as low-power [9], high-resolution [10], [11], [12], or high-speed SAR converters [13]. This method is also implemented in hybrid structures like pipelined SAR ADCs [15]. The extra circuits required for calibration can be as simple as some multiplexors, control logic, and averaging filters [11], [14]. Moreover, as it directly measures the bit weight, this method also converges faster than other calibration schemes based on iterations. With careful design and certain circuit techniques, the overall cycles for calibration can be reduced to less than 1k [11], [12].

For high-resolution SAR converters, however, conventional top-down self-calibration techniques measuring the bit weight error voltage or capacitor mismatch encounter challenges. These techniques usually need an auxiliary DAC with a higher resolution than the main DAC to precisely quantize the error voltage [6], [7], [8], [9]. This usually needs significant hardware overhead. Hence, the bottom-up self-calibration technique [13], which uses lower-weighted capacitors to directly calibrate higher-weighted capacitors, is commonly used in high-resolution SAR converters for its compactness. Up to 16-bit linearity can be achieved by this type of calibration method [10], [11], [12], [15], [16]. Moreover, most conventional top-down self-calibration techniques are based on binary-weighted capacitive DACs, while the bottom-up self-calibration technique can be applied to many nonbinary-weighted SAR or pipeline-SAR ADCs. However, this technique still suffers from the measurement error due to several circuit issues. For example, multiple measurements and averaging are regularly needed to suppress noise during calibration [11], [12], [13], [14], [15], [16], [17], [18], [19]. This could lead to a large number of repetitions depending on the target accuracy (e.g., 512 times for a 12-bit resolution [14]), which is not preferred in applications requiring fast start-up or low-cost probing tests [11], [19].

Up to now, many prior works have discussed the major circuit nonidealities in the self-calibration techniques. However, the analysis normally relies on repeated iterations or simulations [11], [12], [17] and there has been a lack of quantitative analysis of the bit weight error caused by the nonidealities during the calibration. Especially, the mechanism of the noise-induced error is not clear and has

Manuscript received 18 July 2024; revised 5 September 2024; accepted 8 September 2024. Date of publication 19 September 2024; date of current version 24 October 2024. This work was supported by the Hong Kong Government Innovation and Technology Fund under Grant ITS/007/19. (Corresponding author: Yanhang Chen.)

The authors are with the Department of Electronic and Computer Engineering, The Hong Kong University of Science and Technology, Hong Kong (e-mail: ychenjn@connect.ust.hk).

Color versions of one or more figures in this article are available at <https://doi.org/10.1109/TVLSI.2024.3458071>.

Digital Object Identifier 10.1109/TVLSI.2024.3458071

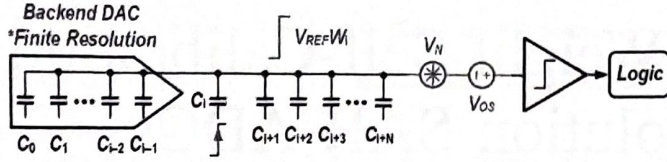


Fig. 1. Self-calibrated SAR ADC with circuit nonidealities.

not been derived in closed-form expressions. Conventionally, it takes a long time to design and simulate at the transistor level to quantify the bit weight error and find the suitable circuit parameters and repetition amount. In this article, we quantitatively analyze the major circuit nonidealities that lead to bit weight error during the self-calibration process. The corresponding circuit-level reduction methods are quantified to provide design insights for designers. Moreover, we develop a statistical model to analyze the noise-induced random bit weight error rising from the self-calibration method. The circuit noise during the self-calibration is analyzed in the calibration process considering other nonidealities like error propagation. The model shows the error mechanism more clearly, and the closed-form expressions obtained from this model help designers conveniently estimate the performance degradation due to the noise during the calibration. The required repetition time based on target ADC specifications can thus be derived from the developed model. Finally, a discussion of practical circuit implementations and design considerations with the developed model is presented to obtain design insight and intuition. The calibration error model is experimentally verified with the design of a 16-bit SAR ADC in a 180-nm CMOS process.

The rest of this article is organized as follows. Section II introduces the fundamental and error sources of the direct bit-weight self-calibration technique. Section III shows a statistical analysis of the noise-induced random bit weight error and the calculation of the repetition time. Section IV verifies our model by measurement results on a 16-bit SAR ADC design. Finally, Section V concludes this article.

II. ERROR SOURCES OF SELF-CALIBRATION TECHNIQUES

The typical diagram and error sources of SAR ADCs with the direct bit-weight self-calibration technique [11], [12], [13], [14], [15], [16] are shown in Fig. 1, where the bit weights of lower-weighted capacitors, $C_{0 \sim (i-1)}$, are assumed error-free and are used as backend DAC to obtain the bit weights of the higher-weighted capacitors. The calibration starts from C_i to the most-significant-bit (MSB) capacitor C_{i+N} . During the calibration of C_i , the bottom plate of C_i is set high, and all the higher-weighted capacitors are grounded (or connected to the common-mode voltage). The DAC voltage after this operation can be derived as

$$V_{DAC} = \frac{C_i}{C_{total}} V_{REF} = W_i V_{REF} \quad (1)$$

where C_{total} is the equivalent total capacitance of the capacitive DAC and W_i is the bit weight of C_i . The backend DAC will then be used to quantize the DAC voltage to obtain W_i , which

can be derived as

$$\sum_{j=0}^{i-1} W_j B_j = W_i \quad (2)$$

where B_j (± 1) are the lower-weighted bits. It is noteworthy that the total weights of the backend DAC should be larger than W_i to guarantee (2) can be met. This requirement also stands for the calibration of higher capacitors, which can be summarized as

$$W_i < \sum_{j=0}^{i-1} W_j. \quad (3)$$

This is also commonly required in high-resolution SAR ADCs as redundancy [11], [12], [13], [14]. After C_i is obtained, it will also be added to the backend DAC to calibrate C_{i+1} using $C_{0 \sim i}$. This process repeats recursively toward the MSB capacitor C_{i+N} . As summarized in prior works, since the switch control and SAR logic can be reused during calibration, the calibration control logic can be area-efficient [11], [12], [14], [19]. This calibration scheme also benefits from fast calibration [11] and compatibility among different redundancy implementations [11], [14], [15].

In the practical circuit implementation, however, several circuit nonidealities limit the calibration accuracy in high-resolution SAR ADC, as shown in Fig. 1. As discussed in prior works, the most significant nonidealities are the comparator offset voltage [7], [8], [9], [11], [13], [14], [15], [16], [17], [18], [19], [20], error of backend DAC [11], [13], quantization error [11], [13], [20], [21], and the random bit weight error caused by circuit noise [6], [9], [11], [12], [13], [14], [15], [16], [17], [18], [19]. These nonidealities are analyzed below.

A. Comparator Offset

During the normal conversion of the SAR ADCs, the offset voltage will not degrade the linearity. Moreover, it can be easily addressed at the system level [14]. During the self-calibration, however, the offset voltage could be sampled in the calibrated bit weights and lead to bit weight errors. If the comparator has an offset voltage V_{OS} , (2) can be rewritten as

$$W_i = \sum_{j=0}^{i-1} W_j B_j + \frac{V_{OS}}{V_{REF}}. \quad (4)$$

After the calibration, all weights except $W_{0 \sim (i-1)}$ carry this offset voltage and its propagated error. Meanwhile, a large offset voltage may also saturate the redundancy range so (3) may become invalid for some bits [11], [13], [15], [19]. Therefore, the comparator offset must be kept very low (1-LSB offset can cause huge errors) for high-resolution SAR converters.

For the offset voltage smaller than the redundancy range, a typical and efficient calibration method is to generate two opposite codes followed by a subtraction [11], [13], [16], [18].

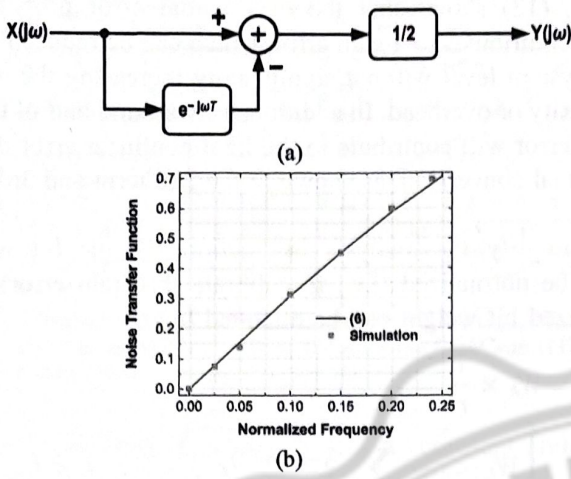


Fig. 2. (a) Block diagram and (b) frequency response of using two opposite codes to cancel offset.

This method can be derived as

$$\begin{aligned} W_i &= \frac{W_{i,\text{set1}} - W_{i,\text{set0}}}{2} \\ &= \frac{W_{i,\text{ideal}} + V_{\text{OS}} - (-W_{i,\text{ideal}} + V_{\text{OS}})}{2} \\ &= W_{i,\text{ideal}} \end{aligned} \quad (5)$$

where $W_{i,\text{set1}}$, $W_{i,\text{set0}}$, and $W_{i,\text{ideal}}$ are the calibrated bit weights when C_i is set high or low, and the correct bit weight of C_i , respectively. The offset voltage can be canceled by digital subtraction. In essence, this method can be modeled as the correlated double sampling (CDS) operating in the digital domain [22]. Hence, it can also suppress low-frequency noise from the converter, such as the flicker noise. Fig. 2(a) shows the equivalent block diagram of this scheme. T is the duration of one calibration cycle and $X(j\omega)$ and $Y(j\omega)$ are the input and output noise magnitudes, respectively. The low-frequency noise transfer function of this system is given by

$$\left| \frac{Y(j\omega)}{X(j\omega)} \right| = \frac{1}{2} \sqrt{2 - 2 \cos \omega T} = \frac{1}{2} \sqrt{2 - 2 \cos \frac{2\pi f}{f_c}} \quad (6)$$

where f is the frequency of noise and f_c is the clock frequency of the calibration process and equals the reciprocal of T . As shown in Fig. 2(b), this method attenuates the low-frequency noise (in many SAR ADCs, the low-frequency noise is mainly the flicker noise from the comparator) and improves the calibration accuracy. It also shows if the corner frequency of low-frequency noise is high, the period of the calibration process should also be shortened to increase f_c . For white noise like the thermal noise, this method has the same effect as 2-time repeated measurements [11].

B. Noise-Induced Random Error

In practical applications, the ADCs are always noisy. The noise will also be sampled into the bit weights during the calibration process, degrading the calibration accuracy. To suppress this random error, repeated measurements and averaging are regularly used [6], [9], [11], [12], [13], [14], [15], [16], [17], [18], [19]. To analyze the averaging method, the calibrated bit weight, W_i , after n -time repeated

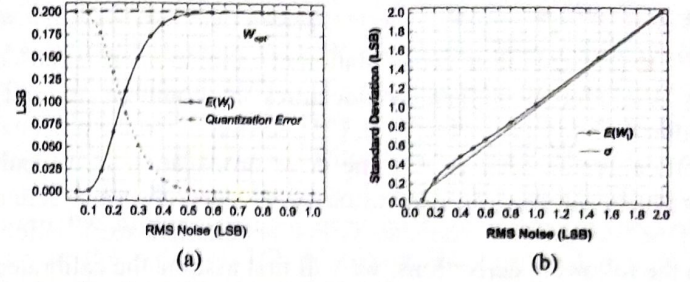


Fig. 3. Simulated (a) mean and (b) variance of the calibrated bit weight versus noise magnitude during calibration.

measurements can be modeled as a random variable with the following mean and standard deviation:

$$E(W_i) = W_{i,\text{ideal}} \quad (7)$$

$$\sigma_{W_i} = \frac{\sigma}{\sqrt{n}} \quad (8)$$

where $W_{i,\text{ideal}}$ is the actual bit weight and σ is the standard deviation of the circuit noise (i.e., root-mean-square or rms noise). If the circuit noise from the comparator and the DAC is large compared to LSB, (8) shows a high number of averaging is needed to suppress the noise down to the required accuracy. The analysis of this effect will be given in more detail later in this article.

C. Quantization Error

As shown in Fig. 1, since the backend DAC stage only has finite numbers of capacitors, its resolution is finite, which introduces the quantization error to the calibrated bit weights [20]. Unlike noise, the quantization error cannot be removed by multiple measurements and averaging alone. Contrarily, it can be reduced by a sufficiently high noise which spreads the measurements through a lot of different quantization levels [14]. This method is similar to the dithering technique [15]. The difference is that the quantization error can be reduced directly by the intrinsic circuit noise, while a pseudorandom sequence is normally injected in the dithering technique [15].

In this section, the main target is to analyze and quantify the remaining quantization error with the presence of circuit noise and to find the noise magnitude that is large enough to reduce the quantization error. Fig. 3 shows the simulated relationship between the mean and variance of the calibrated bit weight and the noise magnitude. In this simulation, the actual W_i is set to $D_0 + 0.2$ LSB. When the circuit noise is higher than $0.5 \text{ LSB}_{\text{rms}}$, the mean of W_i becomes very close to μ and σ (quantization error < 1%). Otherwise, a nonnegligible quantization error exists.

According to the simulation, the rms noise magnitude should be at least $0.5 \text{ LSB}_{\text{rms}}$. In practical designs, the circuit noise of an SAR ADC is often higher than $0.5 \text{ LSB}_{\text{rms}}$ [12], [13], [14], [16] so that the quantization error normally becomes negligible. To further reduce the quantization error, the resolution during the calibration process can be extended by introducing an auxiliary C-DAC [8], [11], [21]. The stochastic quantization method or statistical residue measurement (SRM) can also reduce the quantization error for calibration [12], [20].

D. Error Propagation

The propagation or accumulation of calibration error caused by the aforementioned nonidealities is common in self-calibration [8], [10], [11], [20], [23], [24], [25]. In the practical self-calibrated SAR ADCs, the error propagation is difficult to obtain the analytic expression as it depends on the actual CDAC design and redundancy. For an intuitive explanation, in the following derivations, we will first assume the calibrated DAC is binary-weighted for simplicity. The error propagation effect in the actual redundant CDACs will be illustrated by the simulations in a later analysis.

As described in [20] and [22], the error during the calibration of the lower-weighted capacitors will propagate to the higher ones. Assume the first calibrated capacitor is C_i , and the MSB capacitor is C_{i+N} , the calibrated bit weight with errors of the capacitor C_{i+n} ($i \leq n \leq N$) can be derived as [20], [22]

$$\begin{aligned} W_{i+n} &= W_{i+n,\text{ideal}} + \varepsilon_{i+n} + \sum_{k=1}^n 2^{n-k} \varepsilon_{i+k-1} \\ &= W_{i+n,\text{ideal}} + \sum_{k=1}^{N+1} \frac{2^{N-k+1} \varepsilon_{i+k-1}}{2^{N-n+1}} - \sum_{k=n+1}^N 2^{-k+n-1} \varepsilon_{i+k} \end{aligned} \quad (9)$$

where $W_{i+n,\text{ideal}}$ is the correct bit weight of capacitor C_{i+n} and ε_{i+n} is the sampled error during the calibration of C_{i+n} .

The overall DAC error caused by the calibration is given by

$$\begin{aligned} \varepsilon_{\text{total}} &= \varepsilon_{i+N} + 2\varepsilon_{i+N-1} + 4\varepsilon_{i+N-2}, \dots \\ &= \sum_{k=1}^{N+1} 2^{N-k+1} \varepsilon_{i+k-1}. \end{aligned} \quad (10)$$

Due to the exponential nature of this series, the error effect can be modeled as a gain error factor as follows:

$$\begin{aligned} r &= \frac{\sum_{j=0}^{i+N} W_{j,\text{ideal}} + \varepsilon_{\text{total}}}{\sum_{j=0}^{i+N} W_{j,\text{ideal}}} \\ &= 1 + \varepsilon_{\text{total}}. \end{aligned} \quad (11)$$

With this factor, (9) can be rewritten as

$$\begin{aligned} W_{i+n} &= W_{i+n,\text{ideal}} + \frac{\varepsilon_{i+n}}{2} + \sum_{k=1}^{N+1} \frac{2^{N-k+1} \varepsilon_{i+k-1}}{2^{N-n+1}} - \sum_{k=n+1}^N 2^{-k+n-1} \varepsilon_{i+k} \\ &= W_{i+n,\text{ideal}} (1 + \varepsilon_{\text{total}}) + \frac{\varepsilon_{i+n}}{2} - \sum_{k=n+1}^N 2^{-k+n-1} \varepsilon_{i+k} \\ &= r \times W_{i+n,\text{ideal}} + \frac{\varepsilon_{i+n}}{2} - \sum_{k=n+1}^N 2^{-k+n-1} \varepsilon_{i+k}. \end{aligned} \quad (12)$$

According to (12), the calibrated weight W_{i+n} can be expressed as r times the ideal weight plus half of its own calibration error ε_{i+1} and the backward propagated error (i.e., error from higher-weighted capacitors). Because the errors from higher-weighted capacitors are attenuated by the factor 2^{-k-n-1} as described in the 3rd term of (12) instead of being exponentially amplified, this term becomes less significant.

Overall, (12) shows that the exponential error propagation mainly contributes to a gain error, which can be reduced at the ADC system level without significantly increasing the circuit complexity or overhead. In addition, only around half of the bit weight error will contribute to the final nonlinear error during the normal conversion, as shown in the 2nd term and 3rd term in (12).

To simplify the analysis in Section III, the bit weight should be normalized (i.e., to calibrate this gain error). The normalized bit weight can be obtained by

$$\begin{aligned} W'_k &= W_k \times \frac{1}{r} \\ &= \begin{cases} W_{k,\text{ideal}} - \sum_{j=k+1}^{i+N} 2^{-(j-k+1)} \varepsilon_j, & k < i \\ W_{k,\text{ideal}} + \frac{\varepsilon_k}{2r} - \sum_{j=k+1}^{i+N} 2^{-(j-k+1)} \varepsilon_j, & k \geq i. \end{cases} \end{aligned} \quad (13)$$

As discussed, the above derivations are based on the binary-weighted CDAC. In the practical self-calibrated SAR ADCs, however, the CDAC is usually redundant to accommodate circuit nonidealities during calibration as derived in (3). With CDAC redundancy, the error is not simply propagating with a radix of 2. Therefore, it is relatively difficult to find the analytic expression for the error propagation as it highly depends on the CDAC redundancy.

For general CDACs including the binary CDACs, if all bit decisions are independent for each input level (i.e., random input signal), the overall distortion power during the normal conversion due to the bit weight error can be modeled as

$$P_{\text{dis}} = \sum_{j=i}^{i+N} G_{\text{error},j}^2 \varepsilon_j^2 = \frac{\overline{G_{\text{error}}^2} \overline{\varepsilon^2}}{N+1} \quad (14)$$

where P_{dis} , $G_{\text{error},j}$, ε_j , $\overline{G_{\text{error}}}$, and $\overline{\varepsilon}$ are distortion power during the normal conversion, error coefficient of the calibration error for capacitor C_j , calibration error of capacitor C_j , rms error coefficient, and rms calibration error, respectively. For the error that remains unchanged during the calibration process (e.g., circuit noise), ε_j for each capacitor C_j equals to $\overline{\varepsilon}$. The study (14) shows that the overall distortion power can be simplified using the rms error coefficients.

Fig. 4, where the error is a random circuit noise following normal distribution, shows the simulated $G_{\text{error},j}$ for each individual capacitor and the overall P_{dis} in different self-calibrated nonbinary DACs [11], [18], [26], [27]. Due to redundancy, $G_{\text{error},j}$ varies with different capacitors. However, as depicted in Fig. 4(b), even for CDACs with larger redundancy and many redundant bits [11], [18], [26], [27], $\overline{G_{\text{error}}}$ is only slightly higher than the binary-weighted CDAC. This is because the error propagations in these CDACs are still proportional to the nonbinary bit weights, which are the same as the binary-weighted CDACs. Therefore, for many commonly used nonbinary CDACs, the following can be obtained:

$$\sum_{j=i}^{i+N} G_{\text{error},j}^2 \varepsilon_j^2 = \frac{\overline{G_{\text{error}}^2} \overline{\varepsilon^2}}{N+1} = k_{\text{error}}^2 \frac{\overline{G_{\text{error},\text{binary}}^2} \overline{\varepsilon^2}}{N+1} \quad (15)$$

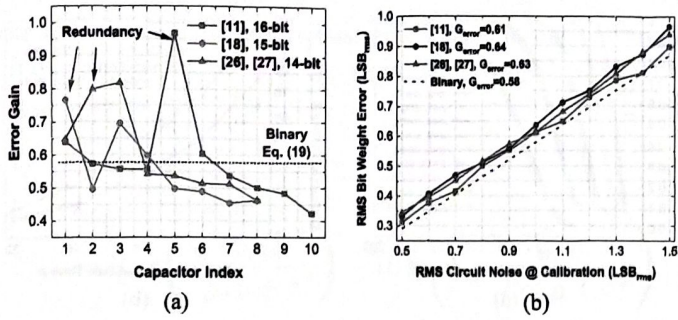


Fig. 4. Simulated (a) $G^2_{error,j}$ for each capacitor and (b) $\overline{G_{error}}$. The numbers of the calibrated capacitors are 10, 8, and 8 for the CDACs in [11] and [18] and [26] and [27], respectively.

where k_{error} and $\overline{G_{error,binary}}$ are a constant related to the practical nonbinary CDAC (normally around 1.1–1.2) and the overall error coefficient for a standard binary CDAC, respectively. As a result, the conclusions obtained from (12) and (13) also hold for redundant CDACs (i.e., the propagated errors mainly lead to a gain error and around 0.5–0.6 of the error during calibration will be transferred to the final rms bit weight errors).

III. STATISTICAL MODELING OF BIT WEIGHT ERROR

As discussed, the random noise's presence helps reduce the quantization error during the bit-weight calibration. However, it introduces measurement error to the bit weight, which increases the distortion during the normal conversion. The noise-induced random bit weight error is modeled below.

A. Modeling of the Bit Weight Error

During the calibration, the noise will be sampled into the calibrated bit weights. After the calibration, each calibrated bit weight will carry an error. The calibrated bit weight can be expressed as

$$W_i = W_{i,ideal} + W_{ei} \quad (16)$$

where W_i , $W_{i,ideal}$, and W_{ei} are the calibrated bit weight of capacitor C_i , the correct bit weight of capacitor C_i , and the sampled bit weight error, respectively. In this section, we mainly study the overall distortion power during the normal conversion, as it is generally the focus of the circuit designers. During the normal conversion of the SAR ADCs, the voltage error due to calibration of any code from a self-calibrated SAR ADC can be given by [6]

$$V_{error} = V_{REF} \times \sum_{j=0}^{i+N} B_j W_{ei} \quad (17)$$

where B_j is the digital bit of capacitor C_j (± 1) and we assume C_i is the first calibrated capacitor as the above derivations. Therefore, the distortion power during the normal conversion will be the variance of (17), i.e.,

$$\begin{aligned} P_{dis} &= V_{error,rms}^2 = V_{REF}^2 \times \text{Var} \left(\sum_{j=0}^{i+N} B_j W_{ei} \right) \\ &= V_{REF}^2 \times \left[\sum_{j=0}^{i+N} W_{ei}^2 + \sum_{j \neq i} W_{ei} W_{ej} \text{Cov}(B_j, B_i) \right] \end{aligned} \quad (18)$$

where $\text{Cov}(B_j, B_i)$ is the covariance between bit B_j and B_i . As derived in Section II-D, $W_{e,i}$ is caused by the noise during the calibration of C_i and the propagated error from other capacitors. Assuming the error during the calibration of C_i is ε_i , (12) shows that for capacitor C_{i+n} in the CDAC, the error coefficient for ε_{i+n} is around 0.5. For the propagated error from the higher-weighted capacitors, their error coefficients are in the radix of 1/2. Moreover, as illustrated in Fig. 4, for the practical nonbinary CDACs, the error coefficient could vary for different capacitors.

Without losing the generality, the bit weight error for C_i can be expressed as

$$W_{ei} = \alpha_i \varepsilon_i - \sum_{j=i+1}^{i+N} \alpha_{i,j} \varepsilon_j \quad (19)$$

where ε_i , α_i , and $\alpha_{i,j}$ are the error (in this section, circuit noise during the calibration is mainly studied so that ε_i can be modeled as random circuit noise) during the calibration of C_i , the error coefficient from ε_i to ε'_i and the error coefficient from higher-weighted capacitor ε_j to ε'_i , respectively. As shown in (13), the errors from the higher-weighted capacitors are exponentially attenuated. Simulations show that this also stands for nonbinary CDACs. Therefore, the 2nd term in (19) can be simplified to only consider the adjacent error propagation (the error from higher weighted capacitors can be derived similarly as well), i.e.,

$$W_{ei} \approx \alpha_i \varepsilon_i - \alpha_{i,i+1} \varepsilon_{i+1}. \quad (20)$$

Substituting (20) into (18), the distortion power during the normal conversion can be therefore obtained as

$$\begin{aligned} P_{dis} &= V_{error,rms}^2 \\ &= V_{REF}^2 \times \left(\underbrace{\sum_{j=i}^{i+N} A_j \varepsilon_j^2}_{\text{Chi-Square Term}} + \underbrace{\sum_{i,k,k} C_{jk} \varepsilon_j \varepsilon_k}_{\text{Correlated Term}} \right) \end{aligned} \quad (21a)$$

$$A_j = \alpha_j^2 + \alpha_{j-1,j}^2 - 2\alpha_j \alpha_{j-1,j} \text{Cov}(B_j, B_{j-1}) \quad (21b)$$

$$C_{jk} \approx \begin{cases} -2\alpha_j \alpha_{j,k} + 2\alpha_j \alpha_k \text{Cov}(B_j, B_k), & k = j+1 \\ 0, & k \neq j+1. \end{cases} \quad (21c)$$

In (21c), as the covariance is only significant for the adjacent bit, the covariances when $k \neq j+1$ are neglected for simplicity.

B. Chi-Square Modeling of rms Bit Weight Error

Although simulations can find out the results for (21), it is too complicated and needs excessive iterations. More importantly, it cannot provide the designers with simple explanations and design intuition. In the practical self-calibration, however, several observations and assumptions can be used to simplify (21) as follows:

- 1) *Normal Distribution*: Regularly, the circuit noise during calibration can be modeled as a random error following

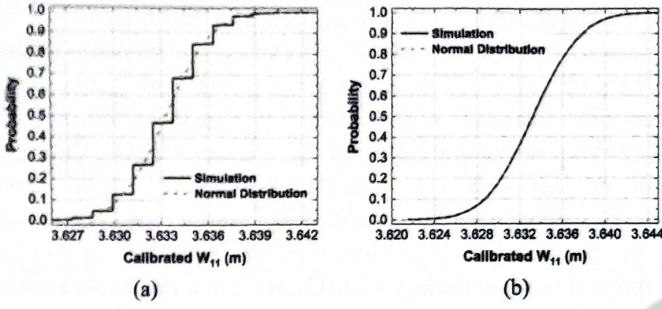


Fig. 5. (a) Simulated CDFs of calibrated W_{11} when the circuit noise is $0.1 \text{ LSB}_{\text{rms}}$ and (b) simulated averaged calibrated W_{11} when the circuit noise is $0.5 \text{ LSB}_{\text{rms}}$ and the calibration repetition time is 32.

the normal distribution. However, when sampled in the calibrated bit weights, due to the finite resolution of the backend DAC, the distribution of the bit weight error is not the normal distribution and becomes difficult to analyze. In the practical self-calibrated SAR ADCs, however, the distribution of the calibrated bit weighted can be approximated as the normal distribution if the circuit noise is high enough and the calibration is repeated sufficient times. First, with the presence of the circuit noise, the quantization error can be decorrelated as analyzed in Section II-C. Therefore, the effect of finite resolution can be reduced by the circuit noise. Moreover, as the calibration typically needs to be repeated many times to reduce the circuit noise during the calibration (from 32-time [11] to over 1000-time [17]), the sampled circuit noise can be approximated as the normal distribution according to the central limit theorem. As shown in Fig. 5, the distribution of the calibrated bit weight will become much closer to the ideal normal distribution with enough circuit noise and calibration repetition time.

- 2) *Quasi-Random bit Decisions*: When deriving (21), the input signal is assumed as a random signal so that the bit decisions during the normal conversion are independent. However, for many practical input signals (e.g., sinusoidal signals), the correlations between different bit decisions are nonzero. Therefore, the correlated term in (21) is also nonzero. However, for a sinusoidal input signal that goes into many different codes, the simulated covariances are less than 0.1 for most bits. Moreover, as the mean of $\varepsilon_i \varepsilon_j$ is 0, its magnitude becomes small as well. Hence, the covariance and the correlated term in (21) can be ignored without introducing to significant error.
- 3) *RMS Error Coefficient*: As shown in Fig. 4 and (14), although the redundancy in the practical CDAC leads to different α_i and $\alpha_{i,j}$ for different bits, the overall error effect is still close to the standard binary CDAC. Therefore, for the overall bit weight error in the entire CDAC, the α_i and $\alpha_{i,j}$ can be unified to the rms error coefficients α_E and α_{EP} . α_E and α_{EP} are the rms error coefficients for all capacitors. According to (15), they are k_{error} -time larger than that in the standard binary-weighted CDACs.

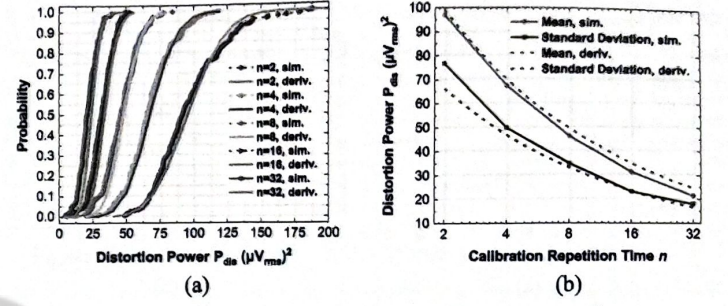


Fig. 6. (a) Simulated and calculated CDFs of $P_{\text{dis}} (V_{\text{error,rms}}^2)$ and (b) simulated and calculated mean and standard deviation of $P_{\text{dis}} (V_{\text{error,rms}}^2)$.

With these observations, (21a) can be simplified to

$$P_{\text{dis}} = V_{\text{error,rms}}^2 \sim V_{\text{REF}}^2 \times \sum_{j=1}^{i+N} (\alpha_E^2 + \alpha_{EP}^2) \varepsilon_j^2$$

$$\frac{V_{\text{error,rms}}}{\sigma'^2} \sim \sum_{j=1}^{i+N} \frac{n V_{\text{REF}}^2 \varepsilon_j^2}{\sigma^2} \quad (22)$$

where

$$\sigma'^2 = \frac{(\alpha_E^2 + \alpha_{EP}^2) \sigma^2}{n} \approx \frac{k_{\text{error}}^2 \left(\frac{5}{16}\right) \sigma^2}{n} \quad (23)$$

where σ' is the equivalent calibration noise, σ is the rms circuit noise during the calibration, k_{error} is a constant related to CDAC defined in (14), and n is repetition time. It is noteworthy that the sum of the squared normal distribution is the chi-square distribution. As discussed, ε_i can be modeled as a random variable following the normal distribution. Hence, (22) can be expressed as

$$\frac{V_{\text{error,rms}}^2}{\sigma'^2} \sim \chi_{(N+1)}^2 \quad (24)$$

where χ_{N+1}^2 is the standard chi-square distribution with a degree of freedom of $N+1$ (i.e., the number of calibrated capacitors). In conclusion, the random calibration error contributed by the noise increases the ADC distortion power by a chi-square distributed random power $V_{\text{error,rms}}^2$ during normal ADC conversions.

Simulations have been performed to verify (24). As shown in Fig. 6, where the CDAC is the same as [11], the reference voltage is 3 V, the k_{error} is 1.1, and the noise during calibration is $0.8 \text{ LSB}_{\text{rms}}$ ($73.2 \mu\text{V}_{\text{rms}}$), the cumulative distribution functions (cdf) of (24) match to the actual simulation well. They also share similar means and standard deviations, indicating that the above simplifications are applicable and will not introduce significant errors.

C. Error Estimation

After considering the noise-induced random bit weight error $V_{\text{error,rms}}^2$, the output power of a calibrated SAR ADC during normal conversions is given by

$$P_{\text{out}} = P_{\text{signal}} + \sigma^2 + P_Q + P_{\text{distortion}} + V_{\text{error,rms}}^2$$

$$= P_{\text{signal}} + \sigma^2 + P_{Q+D} \quad (25)$$

where P_{signal} is the power of input signal, $P_{\text{distortion}}$ is the power of circuit nonlinearity (e.g., settling error), σ is the rms circuit

noise during normal conversions, and P_{Q+D} is the power of both quantization noise and distortion. Hence, the SNDR with $V_{\text{error,rms}}^2$ can be given by

$$\begin{aligned} \text{SNDR} &= 10 \lg \left(\frac{P_{\text{signal}}}{P_{Q+D} + \sigma^2 + V_{\text{error,rms}}^2} \right) \\ &= 10 \lg \left(\frac{P_{\text{signal}}}{P_{Q+D} + \sigma^2} \right) - 10 \lg \left(1 + \frac{V_{\text{error,rms}}^2}{P_{Q+D} + \sigma^2} \right). \end{aligned} \quad (26)$$

When the bit weight error has not been sufficiently reduced by repetitive measurements, $V_{\text{error,rms}}^2$ becomes much higher than P_{Q+D} . Therefore, (26) can be approximated as

$$\text{SNDR}(\text{dB}) \approx \text{SNDR}_{\text{ideal}} - 10 \lg \left(1 + \frac{V_{\text{error,rms}}^2}{P_{Q+D} + \sigma^2} \right) \quad (27)$$

where $\text{SNDR}_{\text{ideal}}$ equals $10 \lg(P_{\text{signal}}/(P_{Q+D} + \sigma^2))$ is the SNDR without bit weight error. As shown in (27), the random bit weight error decreases the SNDR by $10 \lg(1 + (V_{\text{error,rms}}^2/(P_{Q+D} + \sigma^2)))$. This term needs to be kept small enough (e.g., ≤ 0.1 dB) after calibration. Hence, the required repetition time n for the measurement of each capacitor can be derived to be

$$n \geq \frac{\alpha_E^2 + \alpha_{EP}^2}{10^{\frac{\text{SNDR}_{\text{loss}}(\text{dB})}{10}} - 1} f_{N+1}^{-1}(P) \quad (28)$$

where $f_{N+1}(x)$ is the cdf of the chi-square distribution with the degree of freedom of $N + 1$ (i.e., f_{N+1}^{-1} is the inverse distribution function of the chi-square distribution) and $\text{SNDR}_{\text{loss}}$ is the SNDR degradation (dB) due to bit weight error and P is the target yield (e.g., 99%).

D. Results Discussion

Based on the developed chi-square model, the design considerations for practical circuit implementation can be obtained. For most applications, the SAR ADCs only perform the self-calibration during the power-ON process, after long time operation, or after extreme ambient conditions variations [11]. Therefore, the error of the calibrated bit weights should be kept small enough. However, due to the random nature of the circuit noise, the calibrated bit weights are possible to carry significant bit weight errors even though the calibration has been repeated many times. The distortion power due to such bit weight errors can be described by the chi-square model as

$$\begin{aligned} V_{\text{error,worst}}^2 &= \sigma^2 \times f_{N+1}^{-1}(P) \\ &= \frac{(\alpha_E^2 + \alpha_{EP}^2) \sigma^2}{n} \times f_{N+1}^{-1}(P) \end{aligned} \quad (29)$$

where $V_{\text{error,worst}}^2$ is the worst-case distortion power due to the bit weight error for target yield P . As discussed, the calibrated bit weights should be precise after each calibration. As a result, P is normally set large (3σ -yield when $P = 0.9973$ [11], [12] or even 5σ -yield when $P = 0.9999994$ [11]). Fig. 7(a) shows $V_{\text{error,worst}}^2$ under different n and circuit noise calculated from the chi-square model for 3σ -yield. In this example, a

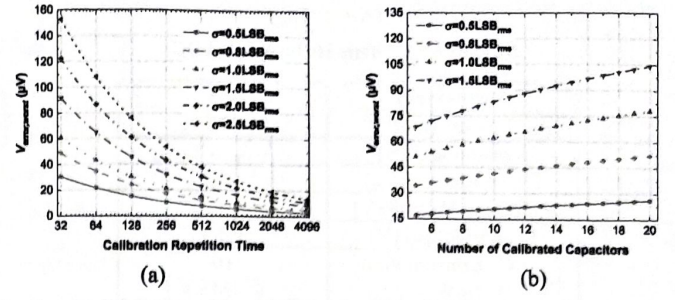


Fig. 7. (a) Worst-case bit weight error under different repetition time n and different noise magnitudes during the calibration. (b) Worst-case bit weight error under different numbers of calibrated capacitors.

16-bit SAR ADC with $V_{\text{REF}} = 3$ V is used for calculation and the number of capacitors for calibration is 15. When the circuit noise is low (around 0.5–0.8 LSB_{rms}), directly increasing the repetition time can effectively suppress the noise during the calibration. Nevertheless, as derived in (8) and (29), the circuit noise is suppressed by the square root of n instead of n . Therefore, increasing n leads to a less effective noise suppression as shown in Fig. 7(a). In some designs, the circuit noise can be higher than 1.0 LSB_{rms} [14] or even 2.0 LSB_{rms} [13], leading to a relatively large n and a long calibration period.

Alternatively, the $V_{\text{error,worst}}^2$ is linearly proportional to the noise magnitude σ during the calibration. Therefore, reducing σ will be more effective than simply increasing n . However, reducing σ may reduce the energy efficiency of the SAR ADCs as it could lead to a quadrate increase in power consumption [12]. Without introducing any extra analog block, the SRM can be used to reduce the noise during the calibration by introducing more comparisons to quantify the bit weights [12], [20]. With SRM, the 3σ -yield worst case of the spurious-free dynamic range (SFDR) is higher than 100 dBc with only 64-time repetition [12]. Additionally, the chi-square model shows that reducing the number of calibrated capacitors can also suppress the noise during the calibration. Nonetheless, the mismatch of noncalibrated capacitors should be reduced, at the cost of higher CDAC capacitance or larger chip area to reduce the capacitance mismatch. An alternative method is to calibrate the lower-weighted capacitors with another comparator connected to the lower section directly [11]; therefore, the noise contribution of the lower-weighted can be reduced. This is equivalent to reducing the number of calibrated capacitors as shown in Fig. 7(b).

IV. EXPERIMENTAL VERIFICATION

A. Measurement Setup

In the previous analysis, the developed model is verified by simulations. However, the circuit nonidealities in the practical implementation could introduce errors and affect the model accuracy. Therefore, the derivation in previous sections is verified in a 16-bit SAR ADC prototype [11]. Its chip micrograph is shown in Fig. 8. The DAC is designed with sub-binary weights with an overall radix of 1.803. This 16-bit SAR design is reconfigured to 1 MS/s to verify the calibration. The dual-segmental calibration [11] is first applied to calibrate

TABLE I
SUMMARY OF THE 16-bit SAR ADC

Parameters	
Process (nm)	180
Resolution (bits)	16
Signal Range (V_{ref})	6
Reference Voltage (V)	3
Supply Voltage (V)	1.8/3
Power Consumption (mW)	10
	@4MS/s
Input Capacitance (pF)	7
Unit Capacitance (fF)	54
Estimated Digital Area (mm ²)	0.015
Digital Data width (bit)	24
SNR (dB)	89
SFDR (dBc)	103
DNL (LSB)	+0.2/-0.2
INL (LSB)	+1.0/-1.0

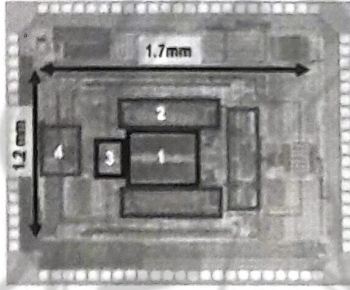


Fig. 8. Chip micrograph of the 16-bit SAR ADC prototype used to verify the derivations.

C_{5-9} . After that, it is disabled so that the calibration of the remaining capacitors (C_{10} to C_{19}) will be the same as the regular self-calibration. According to (24), $V_{\text{error,rms}}^2$ of this self-calibrated SAR ADC can be modeled as a chi-square distributed with a degree of freedom of 10. The main parameters of this 16-bit SAR prototype are summarized in Table I. Twenty capacitors are used for 16-bit linearity to enable redundancy, which relaxes the settling requirements during the normal conversion.

The measurement setup during calibration of the 16-bit SAR ADC is briefly shown in Fig. 9. The opposite code generation described in Section II-A is applied to reduce the comparator input offset voltage and low-frequency noise. The repetition time of calibration is programmed by the FPGA. The calibrated bit weights will be normalized when calibration is finished to reduce the gain error caused by error propagation. Hence, as shown in Fig. 10 where the reference bit weights are obtained from 64-time calibration, a SFDR of 103.5 dBc and a total harmonic distortion (THD) of 99 dBc can be achieved. Without calibration, the SNDR is limited to around 63 dB due to a large capacitance mismatch [11]. The SNR is slightly higher than [11] as a larger resistance and capacitance have been implemented to filter the noise of the input buffer and the reference voltage is by ADP151 loaded by a larger capacitance of 100 μF .

Since other error sources are reduced, the bit weight error caused by noise dominates when repetition time is not sufficiently large. Hence, the chi-square model derived in Section III can be verified. To verify this model, $V_{\text{error,rms}}$

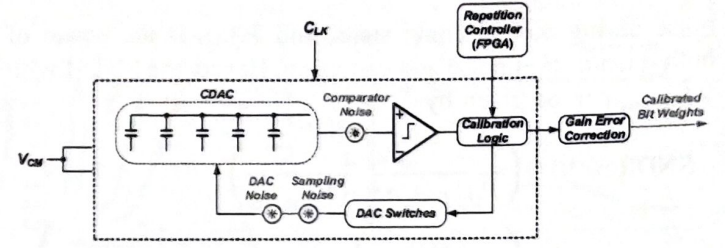


Fig. 9. Summary of the calibration setup and error sources.

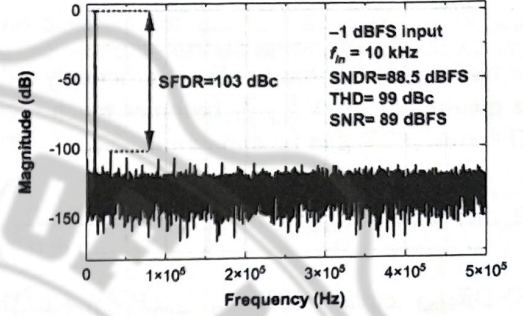


Fig. 10. Measured spectrum without calibration and with the reference bit weights.

defined in (18) needs to be obtained. Fig. 11(a) shows the $V_{\text{error,rms}}$ extraction during the measurement, where two different sets of noise and distortion powers, $P_{N+D,\text{Cal}}$ and $P_{N+D,\text{ref}}$, are obtained from the fast Fourier transform (FFT) spectra. Because the distortion power is small with the reference bit weights, $P_{N+D,\text{ref}}$ is dominated by quantization noise and circuit noise, i.e.,

$$P_{N+D,\text{ref}} = P_Q + \sigma^2 + P_{\text{distortion}} \approx P_Q + \sigma^2 \quad (30)$$

where P_Q , σ^2 and $P_{\text{distortion}}$ are the power of the quantization noise, the power of the circuit noise, and distortion power, respectively. From the same output codes, $P_{N+D,\text{Cal}}$ contains the same P_Q and σ^2 as $P_{N+D,\text{ref}}$. It also includes the random bit weight error power $V_{\text{error,rms}}^2$ and it's given by

$$P_{N+D,\text{Cal}} \approx P_Q + \sigma^2 + V_{\text{error,rms}}^2 \quad (31)$$

The random bit weight error power $V_{\text{error,rms}}^2$ defined in can be calculated as

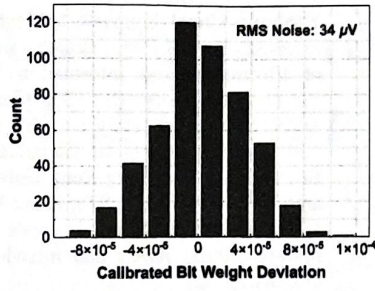
$$V_{\text{error,rms}}^2 \approx P_{N+D,\text{Cal}} - P_{N+D,\text{ideal}} \quad (32)$$

To get the statistical information of $V_{\text{error,rms}}^2$, the calibrations are repeated for 200 runs under each repetition time.

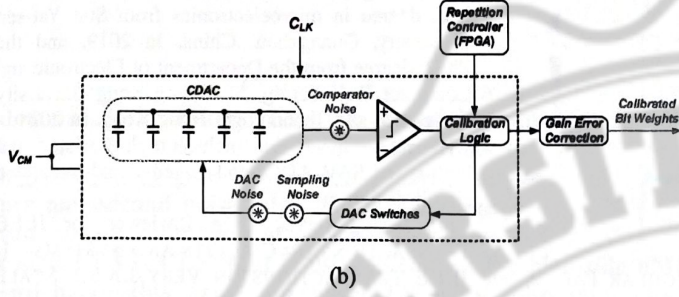
To verify the chi-square model, another required parameter is the circuit noise during the calibration. This is obtained by measuring the calibrated bit weight distribution. As shown in Fig. 11(b), since the opposite code generation is equivalent to two-time repetitive measurements as described in Section II-A, the effective circuit noise during calibration is around 48 μV_{rms} in this measurement setup.

B. Results Comparisons

To verify the statistical error model (i.e., $V_{\text{error,rms}}^2$ follows the chi-square distribution), the cdf, statistical expectation, μ_{error} , and standard deviation σ_{error} of measured $V_{\text{error,rms}}^2$ are compared with the chi-square distribution.

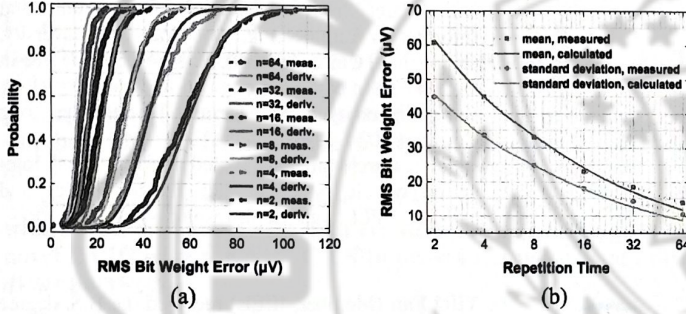


(a)



(b)

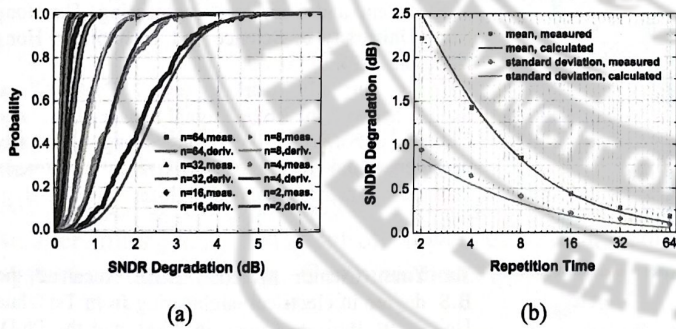
Fig. 11. (a) Measurement setup of bit weights error power and (b) measured histogram of calibration error with opposite code generation.



(a)

(b)

Fig. 12. (a) Measured and theoretical CDFs of and (b) mean values and standard deviations of rms bit weight error with different repetition times.



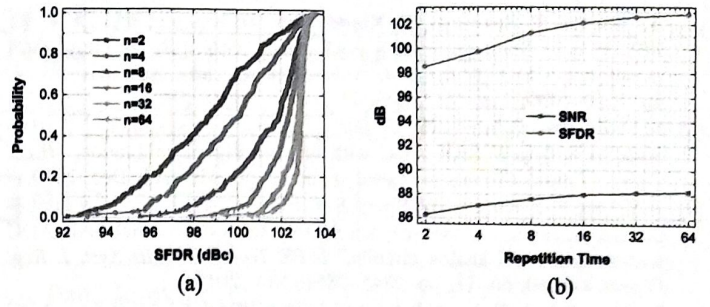
(a)

(b)

Fig. 13. (a) Measured and theoretical CDFs and (b) mean values and standard deviations of SNDR degradation with different repetition times.

Fig. 12(a) compares the calculated and measured CDFs of $V_{\text{error,rms}}$ of the 16-bit SAR ADC. The theoretical CDFs can be calculated by substituting the repetition time, the circuit noise during calibration, and the degree of freedom (i.e., number of calibrated capacitors) into (24). As shown in Fig. 12(a), the measured data matches the calculation from our model. Fig. 12(b) also compares the theoretic and measured mean values and standard deviations of the bit weight error. Corresponding to Fig. 7(a), the measured bit weight error drops slower as n grows exponentially.

As derived in (27), the distribution of SNDR degradation can also be derived by substituting the chi-square distribution in the logarithmic term. Fig. 13 shows the calculated and



(a)

(b)

Fig. 14. (a) Measured cdf of SFDR and (b) mean values of measured SFDR and SNR.

measured CDFs, mean values, and standard deviations of SNDR reduction caused by the random bit weight error. The measurement also matches the calculation.

Fig. 14 shows the measured SFDR and the SNR for better comparison. Similar to the SNDR, the SFDR and SNR become better with more repetition time.

V. CONCLUSION

This article presents a quantitative analysis of major error sources in common bit weight self-calibration methods of high-resolution SAR ADC designs. The comparator offset, the error of backend DAC, the quantization error, the circuit noise, and the error propagation are mainly analyzed. Reduction techniques for these error sources are also introduced. With these errors suppressed properly, the random bit weight error caused by the circuit noise can become the dominant SNDR bottleneck for high-resolution SAR ADCs.

To model the noise-induced random error, a statistical model of the bit weight estimation has been developed. The statistical analysis shows that the circuit noise will be sampled in the calibrated bit weights following the chi-square distribution. Based on this model, the required repetition time of bit weight measurements can also be derived.

The error model is experimentally verified by a 16-bit SAR ADC design in a 180-nm CMOS process. The measurement matches the results from our analysis and the chi-square error model well.

REFERENCES

- [1] C.-C. Liu, S.-J. Chang, G.-Y. Huang, and Y.-Z. Lin, "A 10-bit 50-MS/s SAR ADC with a monotonic capacitor switching procedure," *IEEE J. Solid-State Circuits*, vol. 45, no. 4, pp. 731–740, Apr. 2010.
- [2] Y. Zhu et al., "A 10-bit 100-MS/s reference-free SAR ADC in 90 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 45, no. 6, pp. 1111–1121, Jun. 2010.
- [3] P. J. A. Harpe et al., "A 26 μ W 8 bit 10 MS/s asynchronous SAR ADC for low energy radios," *IEEE J. Solid-State Circuits*, vol. 46, no. 7, pp. 1585–1595, Jul. 2011.
- [4] W. Liu, P. Huang, and Y. Chiu, "A 12-bit, 45-MS/s, 3-mW redundant successive-approximation-register analog-to-digital converter with digital calibration," *IEEE J. Solid-State Circuits*, vol. 46, no. 11, pp. 2661–2672, Nov. 2011.
- [5] M. Ding, P. Harpe, Y.-H. Liu, B. Busze, K. Philips, and H. de Groot, "A 46 μ W 13 b 6.4 MS/s SAR ADC with background mismatch and offset calibration," *IEEE J. Solid-State Circuits*, vol. 52, no. 2, pp. 423–432, Feb. 2017.
- [6] H.-S. Lee, D. A. Hodges, and P. R. Gray, "A self-calibrating 15 bit CMOS A/D converter," *IEEE J. Solid-State Circuits*, vol. SSC-19, no. 6, pp. 813–819, Dec. 1984.

- [7] A. Shikata, R. Sekimoto, T. Kuroda, and H. Ishikuro, "A 0.5 V 1.1 MS/sec 6.3 fJ/conversion-step SAR-ADC with tri-level comparator in 40 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 47, no. 4, pp. 1022–1030, Apr. 2012.
- [8] M. Yoshioka, K. Ishikawa, T. Takayama, and S. Tsukamoto, "A 10-b 50-MS/s 820- μ W SAR ADC with on-chip digital calibration," *IEEE Trans. Biomed. Circuits Syst.*, vol. 4, no. 6, pp. 410–416, Dec. 2010.
- [9] J.-Y. Um, Y.-J. Kim, E.-W. Song, J.-Y. Sim, and H.-J. Park, "A digital-domain calibration of split-capacitor DAC for a differential SAR ADC without additional analog circuits," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 60, no. 11, pp. 2845–2856, Nov. 2013.
- [10] R. Guan, J. Xue, C. Yang, J. Jin, and J. Zhou, "16-bit 1-MS/s SAR ADC with foreground digital-domain calibration," *IET Circuits, Devices Syst.*, vol. 12, no. 4, pp. 505–513, Apr. 2018.
- [11] Y. Chen, Q. Huang, Y. Fan, Q. Zhao, S. Huang, and J. Yuan, "A 16-bit 4-MS/s SAR ADC with dual-segmental bit weight self-calibration," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 71, no. 9, pp. 3961–3974, Sep. 2024.
- [12] Q. Huang, S. Huang, Y. Chen, Y. Fan, and J. Yuan, "A 16 b 5MS/s 93.7dB-SNDR SAR ADC with a split sampling technique and SRM-assisted self-calibration," in *Proc. IEEE Custom Integr. Circuits Conf. (CICC)*, Denver, CO, USA, Apr. 2024, pp. 1–2.
- [13] J. Shen et al., "A 16-bit 16-MS/s SAR ADC with on-chip calibration in 55-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 53, no. 4, pp. 1149–1160, Apr. 2018.
- [14] W.-H. Tseng, W.-L. Lee, C.-Y. Huang, and P.-C. Chiu, "A 12-bit 104 MS/s SAR ADC in 28 nm CMOS for digitally-assisted wireless transmitters," *IEEE J. Solid-State Circuits*, vol. 51, no. 10, pp. 2222–2231, Oct. 2016.
- [15] A. ElShater et al., "A 10-mW 16-b 15-MS/s two-step SAR ADC with 95-dB DR using dual-deadzone ring amplifier," *IEEE J. Solid-State Circuits*, vol. 54, no. 12, pp. 3410–3420, Dec. 2019.
- [16] B. Chen, M. Maddox, M. C. W. Coln, Y. Lu, and L. D. Fernando, "Precision passive-charge-sharing SAR ADC: Analysis, design, and measurement results," *IEEE J. Solid-State Circuits*, vol. 53, no. 5, pp. 1481–1492, May 2018.
- [17] P. Zhang, W. Feng, P. Zhao, X. Chen, and Z. Zhang, "A 16-bit 1-MS/s pseudo-differential SAR ADC with digital calibration and DNL enhancement achieving 92 dB SNDR," *IEEE Access*, vol. 7, pp. 119166–119180, 2019.
- [18] D. Zhang and A. Alvandpour, "Analysis and calibration of nonbinary-weighted capacitive DAC for high-resolution SAR ADCs," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 61, no. 9, pp. 666–670, Sep. 2014.
- [19] Y.-S. Hu, J.-H. Lin, D.-G. Lin, K.-Y. Lin, and H.-S. Chen, "An 89.55 dB-SFDR 179.6 dB-FoMs 12-bit 1MS/s SAR-assisted SAR ADC with weight-split compensation calibration," in *Proc. IEEE Asian Solid-State Circuits Conf. (A-SSCC)*, Tainan, Taiwan, Nov. 2018, pp. 253–256.
- [20] M. Bagheri, F. Schembari, N. Pourmousavian, H. Zare-Hoseini, D. Hasko, and R. B. Staszewski, "A mismatch calibration technique for SAR ADCs based on deterministic self-calibration and stochastic quantization," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 67, no. 9, pp. 2883–2896, Sep. 2020.
- [21] A. T. Nguyen, J. Xu, and Z. Yang, "A 14-bit 0.17 mm² SAR ADC in 0.13 μ m CMOS for high precision nerve recording," in *Proc. IEEE Custom Integr. Circuits Conf. (CICC)*, San Jose, CA, USA, Sep. 2015, pp. 1–4.
- [22] C. C. Enz and G. C. Temes, "Circuit techniques for reducing the effects of op-amp imperfections: Autozeroing, correlated double sampling, and chopper stabilization," *Proc. IEEE*, vol. 84, no. 11, pp. 1584–1614, Nov. 1996.
- [23] C. C. Lee, C.-Y. Lu, R. Narayanaswamy, and J. B. Rizk, "A 12 b 70MS/s SAR ADC with digital startup calibration in 14 nm CMOS," in *Proc. Symp. VLSI Circuits (VLSI Circuits)*, Jun. 2015, pp. C62–C63.
- [24] H.-S. Lee, "A 12-b 600 ks/s digitally self-calibrated pipelined algorithmic ADC," *IEEE J. Solid-State Circuits*, vol. 29, no. 4, pp. 509–515, Apr. 1994.
- [25] S.-H. Lee and B.-S. Song, "Digital-domain calibration of multistep analog-to-digital converters," *IEEE J. Solid-State Circuits*, vol. 27, no. 12, pp. 1679–1688, Dec. 1992.
- [26] M. J. Kramer, E. Janssen, K. Doris, and B. Murmann, "A 14 b 35 MS/s SAR ADC achieving 75 dB SNDR and 99 dB SFDR with loop-embedded input buffer in 40 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 50, no. 12, pp. 2891–2900, Dec. 2015.
- [27] M. Krämer, "High-resolution SAR A/D converters with loop-embedded input buffer," Ph.D. dissertation, Dept. Elect. Eng., Stanford Univ., Stanford, CA, USA, 2015.



Yanhang Chen (Graduate Student Member, IEEE) received the B.Eng. degree from the School of Electronics and Information Technology, Sun Yat-sen University (SYSU), Guangzhou, China, in 2021. He is currently pursuing the Ph.D. degree with the Department of Electrical and Computer Engineering, The Hong Kong University of Science and Technology (HKUST), Hong Kong, China.

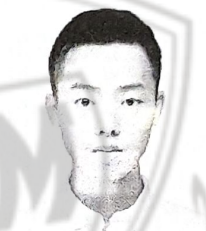
His current research interests mainly include high-resolution ADCs and mixed-signal integrated circuits.



Siji Huang (Student Member, IEEE) received the B.E. degree in microelectronics from Sun Yat-sen University, Guangzhou, China, in 2019, and the Ph.D. degree from the Department of Electronic and Computer Engineering, The Hong Kong University of Science and Technology, Hong Kong, in 2024.

His research interests include high-precision and high-speed SAR ADCs and mixed-signal integrated circuit design.

Dr. Huang serves as a Reviewer for IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—I: REGULAR PAPERS and IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS.



Qifeng Huang (Member, IEEE) received the B.E. degree from the School of Electronic and Information Engineering, Sun Yat-sen University, Guangzhou, China, in 2020, and the Ph.D. degree in electronic and computer engineering from The Hong Kong University of Science and Technology, Hong Kong, in 2024, respectively.

His research interests include mixed-signal integrated circuit systems, such as low-power and low-noise PLLs, and high-resolution ADCs.



Yifei Fan (Member, IEEE) received the B.S. degree in electronic and information engineering (EIE) from The Hong Kong Polytechnic University, Hong Kong, in 2020, and the Ph.D. degree from the Department of Electronic and Computer Engineering, The Hong Kong University of Science and Technology, Hong Kong, in 2024.

He is currently working as a Post-Doctoral Researcher with the Mixed-signal Sensory Integrated Circuits Laboratory, The Hong Kong University of Science and Technology. His research interests include novel biosensors, biomedical instruments, and high-resolution analog-to-digital converters.



Jie Yuan (Senior Member, IEEE) received the B.S. degree in electrical engineering from Tsinghua University, Beijing, China, in 2000, and the Ph.D. degree in electrical engineering from the University of Pennsylvania, Philadelphia, PA, USA, in 2006.

Since 2006, he has been a Faculty Member of the Department of Electronic and Computer Engineering, The Hong Kong University of Science and Technology, Hong Kong, where he is currently a Professor. He is serving as a Post-Graduate Coordinator of the ECE Department and is in charge

of the postgraduate affairs in the ECE Department. His research expertise is in sensory IC design. His research group has made major contributions to the fields of ADC, CMOS imaging sensors, integrated bio-cellular sensing systems, wearable sensors, and energy harvesting.

Dr. Yuan served as the Technical Program Committee Co-Chair of the IEEE Biomedical Circuits and Systems Conference in 2009, the Chair of the Biomedical Circuits and Systems Technical Committee of the IEEE CAS from 2012 to 2014, and the Chair of the Analog Signal Processing Technical Committee of the IEEE CAS Society from 2017 to 2019. He was an Associate Editor of the IEEE TRANSACTIONS ON BIOMEDICAL CIRCUITS AND SYSTEMS and the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—I: EXPRESS BRIEFS, and a Guest Editor of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—I: REGULAR PAPERS.